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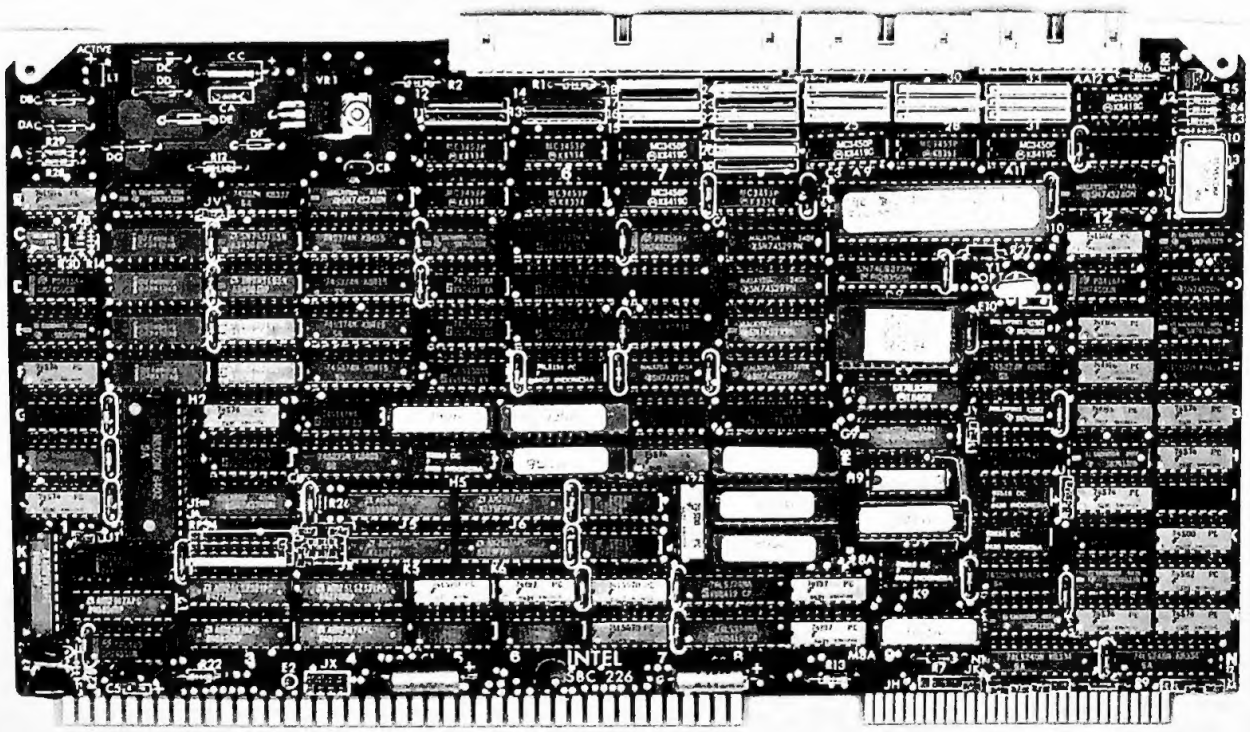
iSBC® 226 STORAGE MODULE DEVICE (SMD) DISK CONTROLLER BOARD HARDWARE REFERENCE MANUAL



Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

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PREFACE

This Hardware Reference Manual describes the iSBC 226 Storage Module Device (SMD) Disk Controller Board. This manual explains how to configure the jumpers and interfaces on the board, and begin programming of the board. It also covers the iSBC 226 Board's installation requirements for a MULTIBUS system environment. For additional information, the following publication is available from the Intel Literature Department:

- Intel MULTIBUS® Specification, Order Number: 98ØØ683

NOTES

Throughout this manual, a slash (/), or an upper-case "L" in parenthesis (L), following a signal name means that the signal is active-low.

When accessing MULTIBUS memory, the iSBC 226 board uses a technique called "Address Relocation". Address Relocation is the addition of two addresses to form a larger physical address. In other Intel manuals, Address Relocation is usually referred to as "Segment" and "Offset".

ACRONYMS

Throughout this manual, acronyms or mnemonics are used to abbreviate multi-word names or functions. Refer to the following list for the acronyms and their corresponding, unabridged spelling.

AFE	Adaptive Format Enable
BWM	Byte Word Mode
CPU	Central processor Unit and/or computer
CSR	Control and Status Register
DMA	Direct Memory Access
ECC	Error Correction Code
EEF	Enable Extended Functions
ESD	Embedded Servo Drive
FIFO	First In First Out (Buffer)
GBSY	Go/Busy Bit
H	Hexadecimal notation for numerical values
(H)	A high level active signal
IOPB	Input/Output Parameter Block
I/O	Input/Output
(L)	A low level active signal
LED	Light Emitting Diode
MB	Mega Bytes
PCB	Printed Circuit Board
RAM	Random Access Memory
SMD	Storage Module Device

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CHAPTER 5 (continued)

TABLES

FIGURES

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CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

The iSBC 226 Storage Module Device (SMD) Disk Controller Board is a high performance disk controller for SMD Interface-compatible disk drives. The iSBC 226 board is a single-height MULTIBUS printed circuit board (see Figure 1-1.). The iSBC 226 board can access up to 16 MB of system memory and control one or two SMD disk drives at data transfer rates up to 2.Ø MB/sec.

This manual provides the installation and setup information needed to interface the iSBC 226 board to one or two SMD disk drives, and integrate it into a MULTIBUS system. Board setup and configuration information is provided in Chapters 2-4. Programming and Operation information is covered in Chapter 5. Bus and interfacing signals information is provided in Chapter 6, with Service Information covered in Chapter 7.

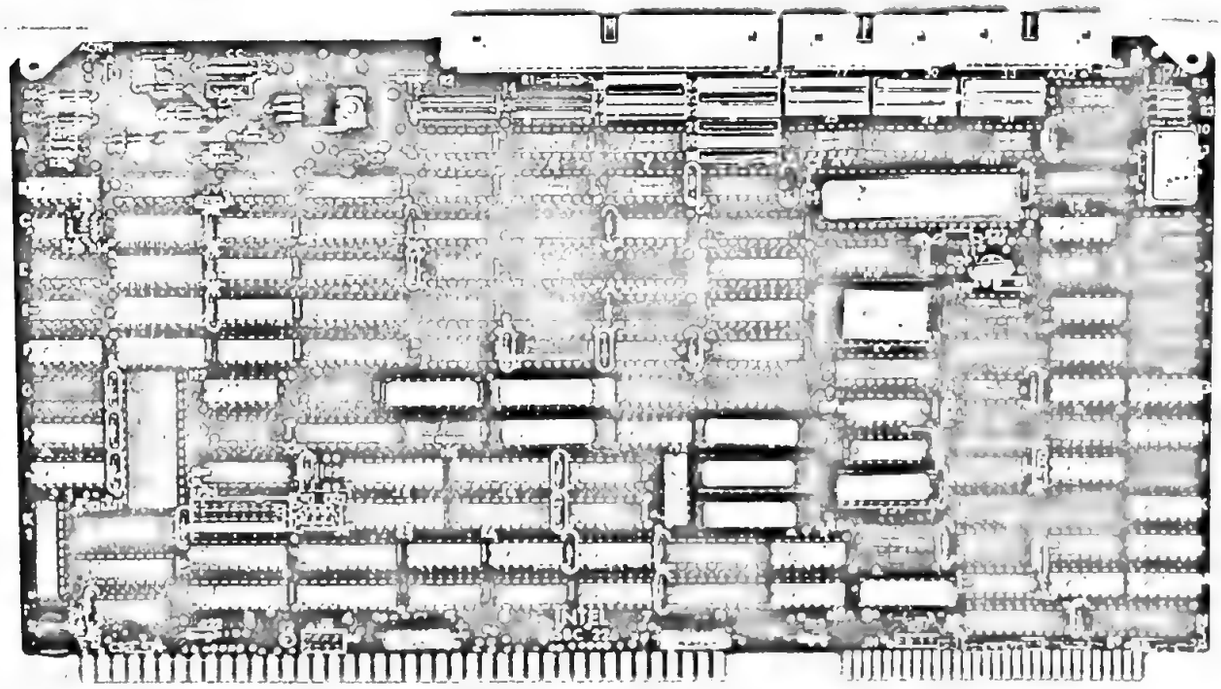

Figure 1-1. iSBC® 226 Storage Module Device (SMD) Disk Controller Board

1.2 GENERAL DESCRIPTION

The iSBC 226 SMD Disk Controller Board interfaces one or two SMD interface compatible disk drives to IEEE 796 MULTIBUS systems. Data transfers are accomplished using DMA, which allows maximum throughput. Drive control is accomplished using I/O Parameter Blocks (IOPBs) and byte I/O registers. See Figure 1-2. for block diagram of the iSBC 266 Board.

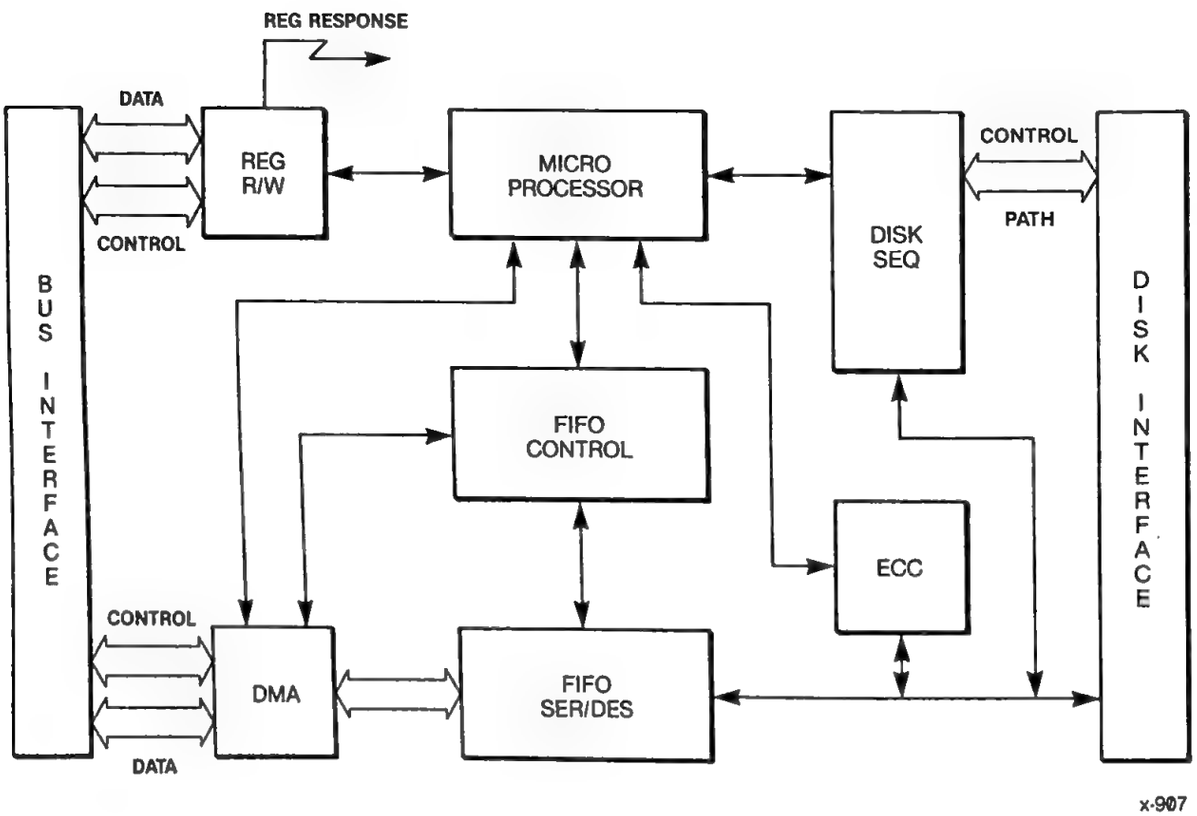

Figure 1-2. iSBC® 226 Board Block Diagram

1.2.1 PROGRAMMABLE FEATURES

The following is a listing of the programmable features of the iSBC 226 board:

- Software controlled 16-bit address bus support.
- Jumper Selectable 2Ø- or 24-bit extended address bus support.
- Software controlled 8- or 16-bit Data Transfers.
- Software controlled Interrupt or Software Polled Operation.
- Software Programmable DMA Throttle
- Software Programmable Drive Size Parameters
- Software Programmable Sector Interleaving

1.2.2 INTERNAL REGISTERS

The use of specific bits within the iSBC 226 board's I/O registers are described in Section 5.4. The iSBC 226 board's internal registers (which are loaded and read by the software driver to establish commands) are listed in Table 5-1.

1.2.3 COMMAND TECHNIQUES

The iSBC 226 board command technique allows command-chaining and concurrent host and Disk Controller operations. Channel control allows a software driver to establish a disk command and parameters in an Input/Output Parameter Block (IOPB) in system memory. The use of specific bits within the IOPBs are described in Section 5.5. IOPB byte definitions are listed in Table 5-2.

The software driver initiates commands, or command chains, by loading the memory address of the IOPB into the iSBC 226 board's Relocation and Address Registers. It then sets the Status Register Bit 7 (Go/Busy Bit - GBSY) to one to initiate the operation. Bit 7 stays set until command (chained) completion or an error is detected.

The iSBC 226 board reads the IOPB from system memory by using Direct Memory Access (DMA) and performs the required function. Upon operation completion or upon detecting an error, the iSBC 226 board writes a completion code into bytes 2 and 3 of the IOPB. To reset the iSBC 226 board at any time, the host Central Processing Unit (CPU) reads the Controller Reset Register.

1.2.4 CHAINED COMMANDS

The iSBC 226 board provides command-chaining capability for complex operations. The software driver can set up a string of commands (e.g., disk-to-disk copy) to allow execution of a series of disk operations, without operating system intervention. At any time, the operating

system can add new IOPBs or remove completed IOPBs from the chain using the attention request protocol. Chained commands allow overlap seek operations on multi-drive subsystems.

1.3 SPECIFICATIONS

General specifications for the iSBC 226 board are listed in Table 1-1. Refer to the INTEL MULTIBUS SPECIFICATION for board AC and DC specifications and MULTIBUS timing information.

Table 1-1. Specifications

Physical Dimensions:	
Packaging:	The iSBC 226 board is a single-height, printed circuit board that plugs into 16-, 20-, or 24-bit address path IEEE 796 bus cardcages.
Width:	30.48 cm (12.0 in)
Height:	17.15 cm (6.75 in)
Shipping Weight:	1400 gm (48.0 oz)
Power Requirements:	
Power:	5VDC ±5% @ 6.2 Amps -12VDC ±5% @ 0.6 Amps
Ground:	Common earth ground must be established between the disk drives, CPU chassis, backplane, and any expansion cabinets.
Environmental Requirements:	
Operating Temperature:	0°C to 55°C (32°F to 130°F)
Operating Humidity:	To 90% relative humidity w/o condensation.
Cooling Requirements:	200 linear feet of airflow per minute per board position at a max. ambient temperature of 55°C.

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Table 1-1. Specifications (continued)

System Related Specifications:	
Transfer Control:	Direct Memory Access (DMA).
DMA Throttle Control:	Programmable throttle value supports any MULTIBUS throughput speed.
Interrupt Priority:	Eight jumper-selectable interrupt levels (INT5* - factory default).
Interrupts:	Non-Bus-Vectored.
Control Technique:	Channel Driven control, Programmable Microprocessor.
Addressing Capability:	16-, 2Ø-, or 24-bit address path.
I/O Parameter Block Length:	24 bytes.
Controller Registers:	Six 8-bit I/O Registers, byte addressable only.
I/O Addressing Capability:	The iSBC 226 board decodes byte addresses for its on-board registers. It responds to either 8- or 16-bit I/O addresses.
Data Transfer Modes:	Data is transferred in bytes or words. Data transfer mode is jumper-selectable.
Data Buffering:	On-board FIFO buffer memory accommodates 2K bytes in word mode and 1K bytes in byte mode.
Sector Size:	1Ø24 bytes.
Data Transfer Limit:	Data transfer length, from 1 to 65,535 sectors.
Software Support:	Standard software driver is RMX-86.
Error Detection and Correction:	A 32-bit Error Correction Code (ECC) is used by the iSBC 226 board. Automatic detection and correction is under software control.

(continued)

Table 1-1. Specifications (continued)

Status LEDs:	Two status LEDs are on the iSBC 226 Board. One LED indicates successful completion of on-board diagnostics. The second indicates when the controller is active.
DMA Data Transfer Rate:	The iSBC 226 board adds less than 5ØØns overhead on each word transferred. Assuming 5ØØns overhead, total transfer time is 1ØØØns for a direct memory access rate of 2.Ø MB/sec. With only 3ØØns of added overhead, the iSBC 226 board can access memory directly at a 2.5 MB/sec rate.
Disk Drive Related Specifications:	
Disk Interface:	Storage Module Device (SMD) interface compatible (up to 2.Ø MB/sec.).
Maximum Disk Capacity:	The iSBC 226 board supports more than 1.2 Gigabytes of on-line storage (drive limited).
Number of Disk Drives:	The iSBC 226 board supports one or two SMD disk drives (any mix of capacities or speeds).
Disk Sector Format:	The iSBC 226 board sector format includes a header field separated from a data field by a splice area.
Header Format:	The header contains sector, head, and cylinder addresses; drive type, and header ECC. Headers are written only during formatting of the media.
Data Verification:	Built-in 32-bit ECC are on the header and data portions of the sector. The ECC detects and corrects error bursts up to 11 bits long, to assure data integrity.

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Table 1-1. Specifications (continued)

Implied Seek Capability:	Data transfer instructions contain an implied-seek command. Data transfers cross sector, head and cylinder boundaries as required (spiral read/write).
Overlapped Seek Capability:	When requests for more than one drive are in chained IOPBs, implicit overlapped seeking may be initiated by the controller.
Disk Data Transfer Rate:	Up to 2.Ø MB/sec on continuous transfers.
Cabling:	Standard SMD flat cabling; one A cable per controller, one B cable per drive.
Dual Port:	Dual port drives are supported.
Defective Sectors: Handling	Defective sectors may be slipped to spare sectors on each track.

1.4 COMPLIANCE LEVEL: IEEE 796 BUS SPECIFICATION (IEEE STANDARD)

All Intel MULTIBUS-compatible boards are designed around the IEEE 796 BUS SPECIFICATION (IEEE STANDARD - formerly the "Intel MULTIBUS Specification"). This standard requires that certain board operating characteristics, such as data bus width and memory addressing paths, be clearly stated in the board's printed specifications (i.e., reference manual). Used properly, this information quickly summarizes the level of compliance the board bears to the published IEEE 796 BUS SPECIFICATION. It clearly states the board's level of compatibility to the MULTIBUS structure. Refer to the IEEE 796 BUS SPECIFICATION or the "Intel MULTIBUS Specification" for additional information.

The following notation states the iSBC 226 SMD Disk Controller board's level of compliance to the IEEE 796 BUS SPECIFICATION:

Master D16 M24 I16 VØL and Slave D8|16

This notation is decoded as follows:

D16 = Represents a data path of 8 and/or 16 bits.
M24 = Represents a 24 bit memory address path.
I16 = I/O address path of 8 or 16 bits.
VØ = Non-Bus-Vectored interrupts are supported.
L = Level-triggered interrupts are supported.
D8|16 = Represents an 8 or 16 bit I/O data path when board functions as a slave.

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CHAPTER 2
BOARD CONFIGURATION

2.1 INTRODUCTION

The following sections describe the procedures used to unpack and configure the iSBC 226 Storage Module Device (SMD) Disk Controller Board.

2.2 UNPACKING AND INSPECTION

Inspect the shipping carton for possible shipping damage. Carefully unpack the iSBC 226 board from its carton. Save the carton and other shipping material for possible later use.

If there is shipping damage, do not unpack the unit. Notify Intel and the freight carrier immediately.

2.2.1 CONTENTS

The shipping carton contains a single, iSBC 226 board. If the iSBC 226 board is damaged, please contact your local Intel Sales Office (refer to Chapter 7 - Service and Repair Assistance).

2.2.2 INSPECTING THE iSBC® 226 BOARD

Inspect the socketed parts on the iSBC 226 board for any that may have loosened during shipment. Ensure that all parts are firmly seated in their sockets. If any parts must be re-inserted, observe proper part orientation.

2.3 CONFIGURING THE iSBC® 226 BOARD

The iSBC 226 board provides several jumper options which can be configured by the customer. These options are described in the following sections. Refer to Appendix A for the factory default jumpers (both user-, and non-user, configurable), and the jumper location diagram.

2.3.1 BASE ADDRESS SELECTION

There are two separate jumper sets used to select the base address. The first set selects response to 8- or 16-bit register addresses. This is controlled by the jumper JA1Ø-JB1Ø.

JA1Ø-JB1Ø installed: 8-bit address
JA1Ø-JB1Ø removed: 16-bit address

The second jumper set (JA/JB 2-9, JE4-JE5, and JC/JD/JR 1-4) selects the actual base address. If 8-bit addressing is selected, the jumpers for address bits Ø-7 are the only valid jumpers, and jumpers for bits 8-F are ignored. Table 2-1 shows how to set the jumpers for several commonly used base addresses.

Use Figure 2-1 and Table 2-1 in configuring the base address to your needs. The jumpers are divided into three groups:

- Jumper blocks JR, JC, and JD control address bits 3 - 6.
- Jumper JE4-JE5 controls address bit 7.
- Jumper blocks JA and JB control address bits 8 - F.

Address bits 3 - 6 are controlled by three jumper blocks JD, JR, and JC. A one on the address line is determined by inserting a jumper between block JR and JC. A zero on the address line is determined by inserting a jumper between block JC and JD. If address bit 3 were to be a zero, then a jumper must be installed between JD (pin 4) and JC (pin 4). If address bit 4 were to be a one, then a jumper must be installed between JC (pin 3) and JR (pin 3).

Address bit 7 is treated the same as bits 8 - F, except that the jumper connection involved is JE pin 4 to JE pin 5. A jumper present asserts a zero on that address line, and conversely, no jumper asserts that line to a one.

Address bits 8 - F are controlled by inserting or removing a jumper between jumper blocks JA and JB. A jumper present asserts that address line to a zero, and conversely no jumper asserts that line to a one. Insert the jumper between similar pin numbers of each block; for example, if address bit D is to be a zero, then a jumper must connect JA pin 6 to JB pin 6.

The iSBC® 226 board is shipped configured for a base address of Ø1ØØH.

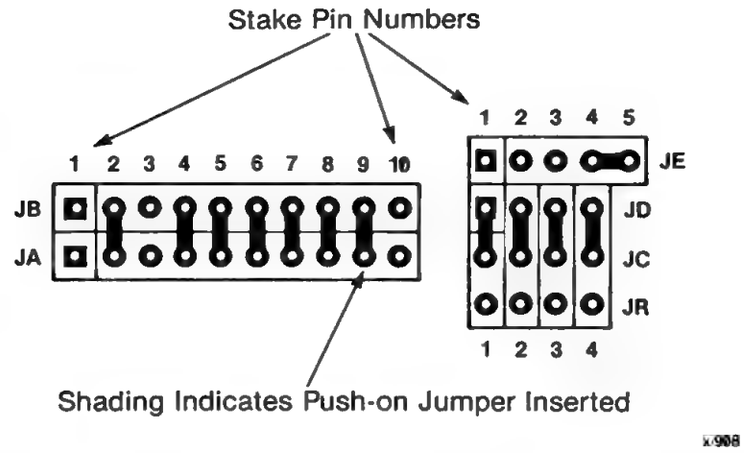

Figure 2-1. Jumper Position for Base Address of Ø1ØØH (Factory Default)

Table 2-1. Jumper Configuration for Base Address

Address Bit:	F	E	D	C	B	A	9	8	7	6	5	4	3	8/16
Pin Numbers:														
Jumper JR/JC/JD										1	2	3	4	
Jumper JE4-JE5									X					
Jumper JA/JB	2	4	6	8	9	7	5	3						1Ø
Address:														
Ø4ØH (8-bit)	X	X	X	X	X	X	X	X	I	RC	CD	CD	CD	I
ØEE4ØH (16-bit)	O	O	O	I	O	O	O	I	I	RC	CD	CD	CD	O
ØØØH (8-bit)	X	X	X	X	X	X	X	X	Ø	CD	CD	CD	CD	I
Ø1ØØH (16-bit)	I	I	I	I	I	I	I	I	O	CD	CD	CD	CD	O

Notes: O = Out
I = In
X = Don't care
RC = Jumper from JR to JC
CD = Jumper from JC to JD
The lower four bits (Ø-3) are represented by one jumper (CD).
The factory default base address is Ø1ØØH.

2.3.2 20-, 24-BIT ADDRESS RELOCATION

The iSBC 226 board can function in systems using 16-, 2Ø-, or 24-bit addressing. The 2Ø-, or 24-bit mode is jumper selectable (see below). The 16-bit mode is software selectable. The status of the jumper can be determined by reading bit 3 of the Control Status Register (CSR). If bit 3 is set, it indicates that the board is jumpered for 24-bit address mode. Both the 2Ø- and 24-bit modes allow 16-bit addressing.

Address Mode	Jumper JM1-JM2	Jumper JM3-JM4
16/2Ø-bit (Default)	Out	In
16/24-bit	In	Out

2.3.3 24-BIT ADDRESS JUMPERS

The iSBC 226 board drives the upper four address lines in the 2Ø-bit address mode. If you require these address lines to float, remove the following factory-installed jumpers:

Address Line	Jumper
ADR14H	JM5-JM6
ADR15H	JK5-JK6
ADR16H	JK1-JK2
ADR17H	JK3-JK4

2.3.4 INTERRUPT REQUEST LEVELS

Any one of eight interrupt request levels can be chosen. The iSBC 226 board is shipped from the factory configured for interrupt request level 5 (INT5/). The selection is made by connecting a wire-wrap jumper from stake pin E2 to the number 3 stake pin on the JX connector block. See Table 2-2 and Figure 2-2 for pin numbers and locations.

Table 2-2. Interrupt Request Levels

Interrupt Request Level	Connect Pin to Pin
INTØ/	E2 JX2
INT1/	E2 JX7
INT2/	E2 JX4
INT3/	E2 JX5
INT4/	E2 JX8
INT5/ (Default)	E2 JX3
INT6/	E2 JX6
INT7/	E2 JX1

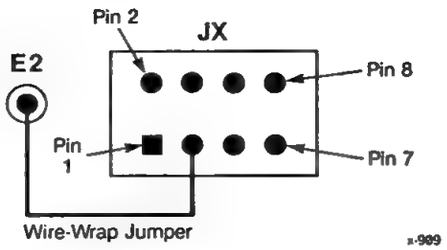

Figure 2-2. Stake Pin E2 and JX Connector Block (Default Configuration)

2.3.5 DISABLE BPRO/ SIGNAL

If the iSBC 226 board is to use parallel DMA arbitration, the BPRO/ signal must be isolated from the MULTIBUS. This can be accomplished by removing jumper JE1-JE2. The iSBC 226 board is shipped configured for serial DMA arbitration.

Serial DMA Arbitration:	Install Jumper JE1-JE2
Parallel DMA Arbitration:	Remove Jumper JE1-JE2

2.3.6 POWER FAIL WARNING

Some MULTIBUS chassis provide power fail warning. This can be implemented by installing jumper JH1-JH2 and providing an appropriate power fail signal on pin 18 of the P2 connector. The signal on pin 18 of the P2 connector must go to ground when the AC power source fails. Using the AC power fail indicator, versus DC, allows the iSBC 226 board more time to protect the drive from accidental spiral writes.

2.3.7 REMOTE ACTIVITY INDICATOR

An on-board LED indicates when the controller is busy. A remote indicator signal is also available to the backplane; install jumper JN1-JN2 and wire the remote LED between +5 volts and pin 42 of connector P2.

2.3.8 FACTORY CONFIGURED JUMPERS

There are several jumpers on the iSBC 226 board which should not be altered because they are configured and installed for factory use only (see Table 2-3 and Appendix A). Most of these jumpers are hard wired, not removable jumpers.

Table 2-3. Factory Configured Jumpers

Jumper	Status	Description
JY2-JY3	In	Closes ECC feedback loop
JY1-JY2	Out	
JJ1-JJ2	Out	Selects Clock for disk sequencer
JJ3-JJ4	In	
JH5-JH6	In	Selects clock for DMA sequencer
JH3-JH4	Out	
JZ1-JZ2	In	Enables crystal clock
JT1-JT2	Out	
JT2-JT3	In	Buffer Memory Configuration
JV2-JV3	In	
JV1-JV2	Out	

2.3.9 SECTOR SIZE AND FIRMWARE

The sector size (1Ø24 bytes) and format type are controlled by parameters contained in PROM which are not user-configurable. Drive type parameters are contained in EPROM and are user-configurable.

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CHAPTER 3
SYSTEM CONSIDERATIONS AND DISK DRIVE PREPARATION

3.1 INTRODUCTION

This chapter discusses system considerations for the iSBC 226 SMD Disk Controller Board, and configuration instructions for disk drives used with the iSBC 226 board. Included in this chapter are: backplane and power considerations, serial and parallel DMA arbitration, and instructions for configuring a disk drive to be used with the iSBC 226 board.

3.2 SYSTEM CONSIDERATIONS

This section provides information on cardcage slot selection, DMA bus arbitration, and power considerations.

3.2.1 CARDCAGE SLOT

The priority arbitration level of the iSBC 226 board is critical and affects which cardcage slot is chosen for board installation. Check your system requirements.

3.2.2 DMA BUS ARBITRATION

The iSBC 226 board accommodates either serial (default configuration) or parallel DMA priority arbitration. Serial arbitration has restrictions on the number of bus masters it can arbitrate (maximum of three). Parallel bus arbitration is more versatile, can handle more bus masters, and is provided standard in many cardcages. As use of serial or parallel bus arbitration is chassis or backplane dependent, consult your systems manual for more information. Set jumper JE1-JE2 as shown for serial or parallel priority arbitration:

Serial DMA Arbitration:	Install jumper JE1-JE2
Parallel DMA Arbitration:	Remove jumper JE1-JE2

3.2.3 POWER CONSIDERATIONS

The iSBC 226 board uses -5 vdc to power the differential drivers/receivers for the SMD interface. The -5 vdc is provided by an on-board regulator supplied from the system -12 vdc.

The iSBC 226 board will affect the power consumption of the entire computer system. Be sure the power supplies are capable of handling the entire power load. A power supply that is just adequate may cause intermittent and unusual problems due to noise generated by occasionally going into overcurrent protection. The iSBC 226 board conforms to the MULTIBUS voltage specifications.

Voltage Limits: 5 volts ± 5% at 6.2 Amps
-12 volts ± 5% at Ø.6 Amps

3.3 DISK DRIVE PREPARATION

The disk drive must be unpacked and configured for use with the iSBC 226 board. Inspect the shipping container of the disk for any shipping damage, and if any, notify the carrier immediately. Unpack the drive and remove any shipping constraints.

Configure the drive for use by the iSBC 226 board. This entails setting up several parameters such as unit select, number of sectors, and ensuring that sector and index pulse are provided on the A cable. Consult the drive manual for the exact method of configuring your drive.

3.3.1 DRIVE UNIT SELECT

Unit select is usually set by either a plug on the front of the drive or by switches on one of the internal circuit cards. The iSBC 226 board can access drives addressed Ø and 1. The first drive connected must be set as Unit Ø.

3.3.2 NUMBER OF SECTORS PER TRACK

The number of sectors per track are typically selected by switches on a circuit card internal to the disk drive. Determine the number of sectors per track by using Table 3-1.

The iSBC 226 board adaptive format requires only 67 bytes of overhead and is more efficient because it does not require the head switching time.

NOTE

Caution must be used when selecting the number of sectors per track in the iSBC 226 board adaptive mode. The drive specification timing for write gate deasserting to read gate asserting must be met. This specification is typically 1Ø micro-seconds for standard SMD drives. Read gate is asserted by the iSBC 226 board eight bytes after a sector pulse. Write gate is deasserted by the iSBC 226 board 7 bytes after the ECC word.

If the sector slip feature is being used, the number of sectors available to the program is the number of allocated sectors less the spare sectors. See Section 5.7.5 for more information on the sector slip feature.

The actual setting of the drive switches may be different than the number of data sectors required. Most disk drives will have a runt sector, that is, a very small sector at the end of the disk. The iSBC 226 board must have all sectors formatted, and sometimes the runt sector is too small to format. This will result in error 19H (illegal sector size), which can be corrected by resetting the sector switches in the drive. If the last sector is too small to be a data sector, but you have included it in the max sector value, then you will also receive error 19H. Consult your drive installation manual for more information concerning runt sectors.

Table 3-1. Maximum Number of Bytes and Sectors Per Track

Bytes Per Track	Sectors Per Track
13,44Ø	12
2Ø,16Ø	18
2Ø,48Ø	18
2Ø,48Ø	18
28,16Ø	25
Data Bytes Per Sector	1Ø24
Media Compatibility	226
Minimum Bytes/Sector †	1Ø91

Note: (†) Not including the write gate to read gate delay required.

3.3.3 SECTOR AND INDEX PULSES

Both the A (Daisy Chain) cable and the B (Radial) cable can provide sector and index pulses. Disk drive vendors usually provide drives with the sector and index pulses on the A cable. The iSBC 226 board requires sector and index pulses to be on the A cable.

3.3.4 DISABLE TAG 4 AND TAG 5

Some disk drives use the spare interface lines for maintenance functions. Other disk drives use the spare interface lines for extended cylinder bits. The iSBC 226 board is designed to utilize the extra lines as cylinder address lines. Therefore the disk drive must be configured to disable Tag 4 and 5.

***

CHAPTER 4
INSTALLATION AND CHECKOUT

4.1 INTRODUCTION

This chapter covers installation considerations and provides instructions for installing, cabling, and performing a checkout of the iSBC 226 Storage Module Device (SMD) Disk Controller Board.

4.2 INSTALLATION CONSIDERATIONS

Installation considerations such as power, cooling, physical size requirements, and interfacing requirements are discussed in the following sections.

4.2.1 POWER REQUIREMENTS

The iSBC 226 board requires 5 vdc (±5%) at 6.2 Amps, and -12 vdc (±5%) at Ø.6 Amps. Common earth ground must be established between the disk drives, the CPU, the backplane, and any expansion cabinets.

4.2.2 COOLING REQUIREMENTS

A minimum airflow of 2ØØ linear feet per minute per board position, at a maximum ambient temperature of 55°C, is required for sufficient cooling.

4.2.3 PHYSICAL DIMENSIONS

The iSBC 226 board is a single-height MULTIBUS printed circuit board measuring 3Ø.48 cm (12.Ø in) wide, by 17.15 cm (6.75 in) in height.

4.3 BOARD INSTALLATION

Place the iSBC 226 board into a 16-, 2Ø-, or 24-bit address path Intel MULTIBUS or IEEE 796 Bus cardcage. Ensure that the board is facing in the proper direction, and that it is firmly seated. Be careful not to dislodge any socketed ICs on the iSBC 226 board.

NOTE

For the initial system check, cable only one disk drive. You can connect another disk drive after initial testing (Section 4.5). Refer to Figure 4-1. for the disk drive cabling diagram.

4.3.1 CONNECT THE A CABLE

Install the A cable (daisy chain), observing Pin 1 markings on both connectors. This cable connects to the center connector (J4) on the iSBC 226 board, and to the A cable connector on the disk drive. If there are two 6Ø-pin connectors on the drive marked IN and OUT, use the IN connector. The other 6Ø-pin connectors on the drive need a terminator on them, or the terminator must be built into the drive. If the drive is dual ported, disable one of the ports.

4.3.2 CONNECT THE B CABLE

Install the B cable (26-pin connector) from any B cable port on the iSBC 226 board to the appropriate connector on the disk drive. The iSBC 226 board's B cable ports are not keyed to the logical disk drive number (ie., drive number Ø can connect to either port of the iSBC 226 board). When installing this cable, ensure that the black stripe on the shielded cable lines up with the pin 1 markings on the connectors for the iSBC 226 board and the drive.

Install a ground braid wire between the ground terminal on the disk drive(s) and the computer system ground. This completes board installation.

4.4 CABLING MULTIPLE DRIVES

If two drives are to be used, the A cables and B cables must be configured differently than with a single drive installation. Refer to Figure 4-1 for cabling diagram.

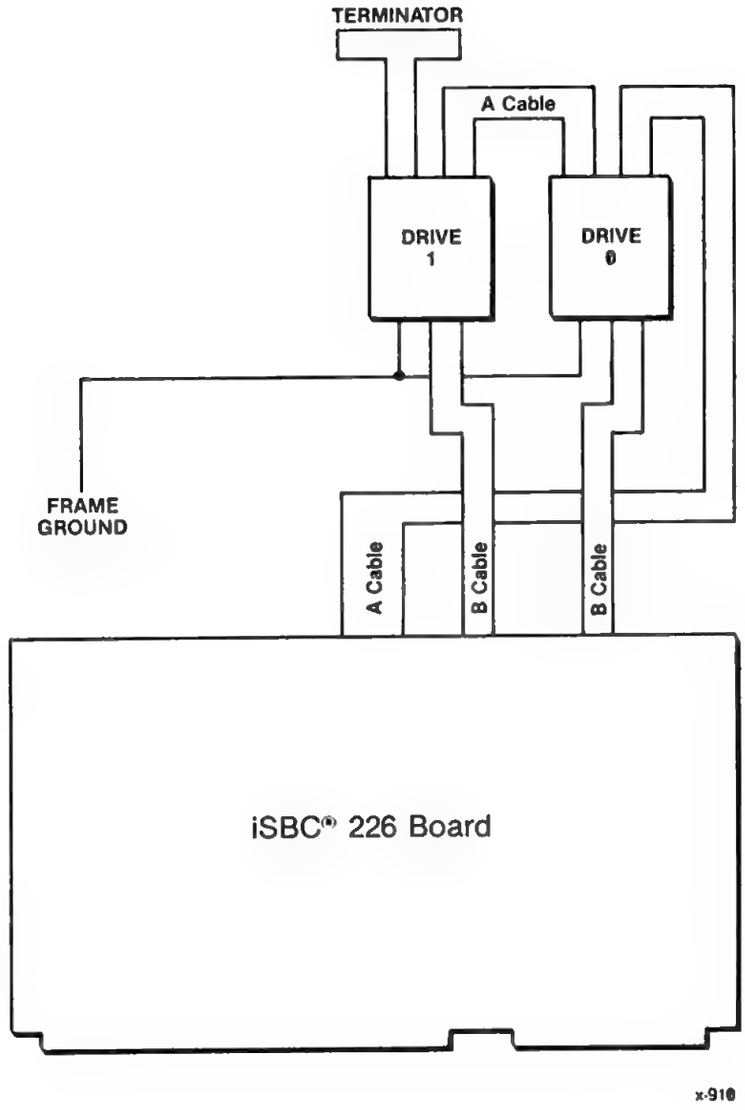


Figure 4-1. iSBC® 226 Board and Disk Drive Cabling Diagram

4.4.1 TERMINATOR

Remove the terminator from the drive currently connected to the controller. Install the terminator on the last drive in the chain.

4.4.2 A CABLE (DAISY CHAIN CABLE)

Connect the A cable from the OUT connector of one drive to the IN connector on the next drive. The maximum total length of all the A cables is 1ØØ feet. Thus, if the cable from the controller to the first drive is 3Ø feet, and the length of the A cable between the drives is 2Ø feet, then the total length is 5Ø feet which is under the maximum allowable.

4.4.3 B CABLE (RADIAL CABLE)

Connect the B cables from each drive directly to a B cable port on the iSBC 226 board. Each B cable may be up to a maximum of 5Ø feet long.

4.4.4 UNIT SELECT

When two drives are connected, be sure to change the unit select numbers for each drive so that they are unique, and that no drive has a unit number greater than 1.

4.5 INITIAL TESTS

This section covers initial testing and relies upon the operator's familiarity with the computer system monitor.

4.5.1 POWER-UP AND SELF TEST

The iSBC 226 board initiates a Self Test upon power-up, which is indicated by the on-board LED. The LED should light up for a brief period and then go off. If it remains on, the board is not functioning properly. Refer to Section 5.6.13 for information on the Self Test command, or contact Intel Customer Support for further help.

NOTE

Check the power supply voltages to insure that they are within limits.

5 vdc (± 5%) at 6.2 Amps
-12 volts (± 5%) at Ø.6 Amps

4.5.2 DRIVE READY TEST

Bring the disk drive up to operating speed and wait for a Drive Ready Status. Read the Reset Register. This resets the iSBC 226 board, selects drive zero, and tests the Drive Ready Status. Read the Control Status Register (CSR) for the results of the Drive Ready test. The CSR should contain Ø1H or Ø9H, denoting whether in 2Ø- or 24-bit address mode.

If bit Ø is not set, re-check the drive cable connections and try again. If still unable to get proper status, check the 12 vdc supply on the MULTIBUS. If the problem persists, check the disk drive for functionality with an off-line tester.

***

CHAPTER 5
PROGRAMMING AND OPERATION

5.1 INTRODUCTION

This section contains the information needed to program and operate the iSBC 226 SMD Disk Controller Board.

5.2 PROGRAMMING TECHNIQUES

Commands for the iSBC 226 board are set up using an I/O Parameter Block (IOPB) in system memory. Refer to Figure 5-1 for an example of an IOPB. The IOPB is an area in system memory used for passing command level information between the iSBC 226 board and the CPU. The CPU writes and reads the IOPB by using normal byte or word instructions. The iSBC 226 board reads and writes the IOPB by using byte mode DMA.

Commands are initiated by loading the starting address of an IOPB into IOPB Pointer registers on the iSBC 226 board controller and setting the Go/Busy bit (GBSY) of the controller Status Register. GBSY stays set until all commands in the IOPB chain are completed or a hard error is detected. Upon completion, the iSBC 226 board writes the corresponding completion codes into bytes 2 and 3 of the IOPB in system memory. Table 5-2 lists the bytes in an IOPB.

The CPU builds the IOPB in system memory with the appropriate information and then passes the address of the IOPB by loading the first four I/O registers. The CPU then sets GBSY in the CSR. The iSBC 226 board transfers the IOPB from memory into the iSBC 226 board at the start of a command. The iSBC 226 board then processes the command and resets the GBSY bit of the CSR on completion. While processing the command, the iSBC 226 board may access the IOPB again, and it may also directly access data to or from memory. IOPBs may also be chained together. When chained, the iSBC 226 board may perform overlap seeks on multiple drives and execute data transfers without CPU intervention.

Each byte in the IOPB has an address relative to the command byte. In order to maintain IOPB integrity, all 24 bytes of allowable IOPB space must be reserved.

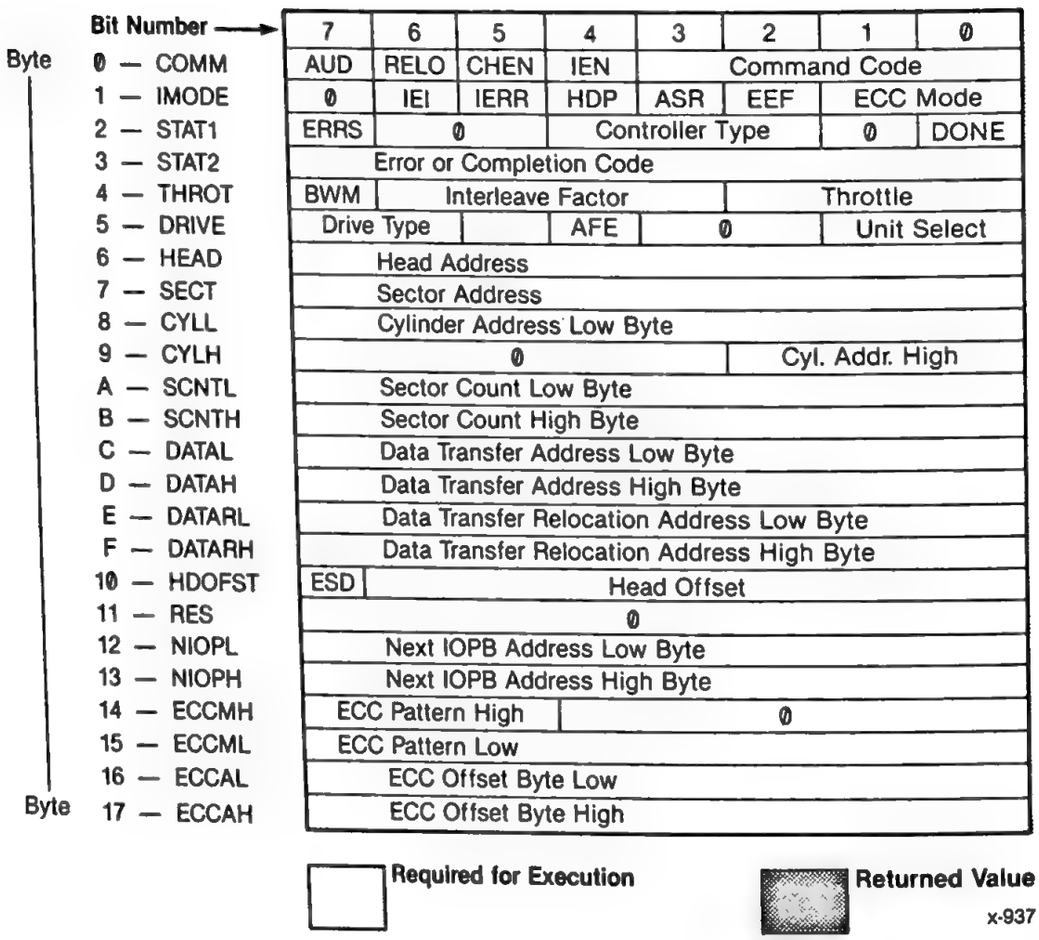


Figure 5-1. Example of Input/Output Parameter Block (IOPB)

5.3 MULTIBUS® ADDRESS RELOCATION

When accessing MULTIBUS memory, the iSBC 226 board uses a technique called Address Relocation. Address Relocation is the addition of two addresses to form a larger physical address. Two types of Address Relocation are supported by the iSBC 226 board: 20-bit address relocation and 24-bit address relocation. Either type of relocation may be used when specifying 16 bits of memory address. For 16-bit memory addressing, the relocation register should be loaded with zero. A jumper on the iSBC 226 board board selects either 20-bit or 24-bit relocation. The position of the 20-bit or 24-bit mode jumper can be determined by examining bit 3 of the CSR.

NOTES

In other Intel manuals, Address Relocation is usually referred to as "Segment" and "Offset".

This manual also refers to both IOPB relocation and data relocation. Do not confuse one with the other. IOPB relocation refers to the address at which an IOPB resides in memory. Data relocation refers to the address at which the data buffer exists. Data relocation may be affected by RELO (bit 6 of Command byte 0), but IOPB relocation will not be affected. The jumper for 20-, 24-bit address selection affects address relocation for both data and IOPB's.

5.3.1 20-BIT ADDRESS RELOCATION

The iSBC 226 board forms a 20-bit physical address by adding a 16-bit address word to a shifted 16-bit relocation word. The relocation word is shifted by four bits as shown in Figure 5-2.

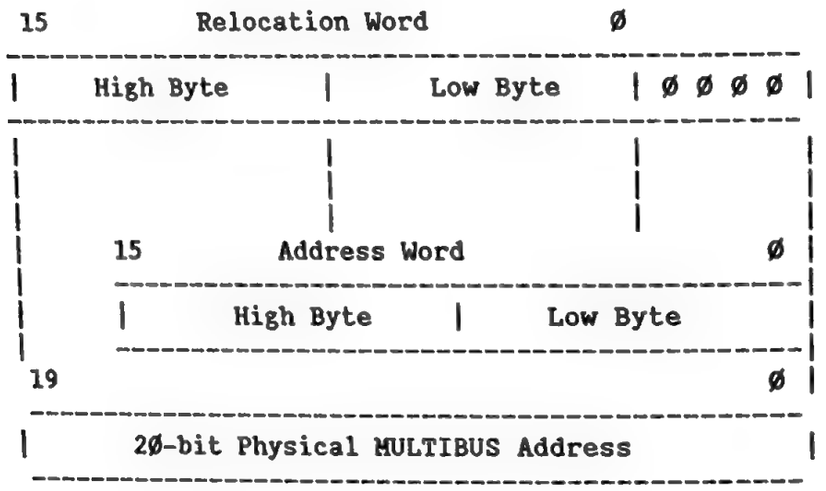


Figure 5-2. 20-Bit MULTIBUS® Address Relocation

5.3.2 24-BIT ADDRESS RELOCATION

For 24-bit address relocation the iSBC 226 board calculates a 32-bit physical address. The address word comprises the least significant 16-bits, and the relocation word becomes the most significant 16-bits. When addressing memory, only the lower 24-bits of the physical address are used. See Figure 5-3.

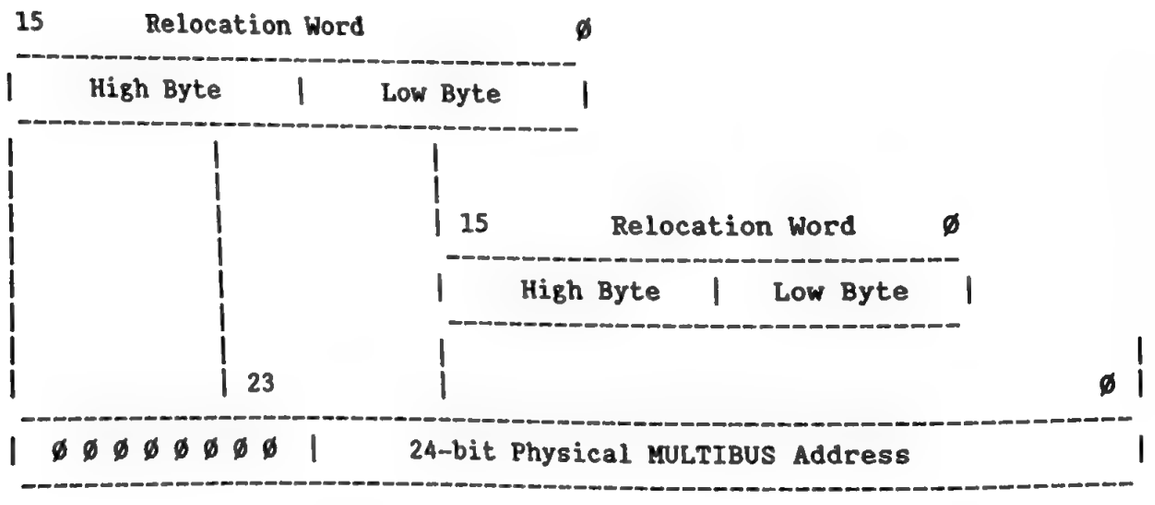


Figure 5-3. 24-Bit MULTIBUS® Address Relocation

5.3.3 IOPB ADDRESS RELOCATION

IOPB relocation occurs whenever a value is loaded into the IOPB relocation registers. The IOPB address registers and IOPB relocation registers are combined to form either a 2Ø-bit or 24-bit physical memory address as shown in Figure 5-2 and 5-3.

When chaining IOPB's, the relocation registers are used in conjunction with the next IOPB address bytes to form a new 2Ø-bit or 24-bit physical MULTIBUS address. This address points to the next IOPB in the chain. All IOPBs in a chain must reside in the same 64K byte segment whose base address is in the relocation registers. The base address is computed by shifting the relocation registers 4 or 16 bits to the left depending on the relocation mode. See Figure 5-2 and 5-3.

5.3.4 DATA TRANSFER ADDRESS RELOCATION

The starting address for a data transfer operation is specified by IOPB bytes ØCH, ØDH, ØEH, and ØFH. If RELO is clear, the data address bytes (IOPB bytes ØDF and ØCF) specify the physical MULTIBUS address for the transfer. If RELO is set, the iSBC 226 board uses bytes ØFH and ØEH as the data relocation bytes and bytes ØCH and ØDH as the data address bytes. Data relocation occurs in the same manner as IOPB relocation. Figure 5-2 and 5-3 shows how data relocation addresses are formed.

5.4 iSBC® 226 BOARD I/O REGISTERS

Table 5-1. iSBC® 226 Board Input/Output Registers

Usage	8-Bit I/O Port Address	16-Bit I/O Port Address
IOPB Relocation Register Low Byte	ØØØH	Ø1ØØH
IOPB Relocation Register High Byte	ØØ1H	Ø1Ø1H
IOPB Address Register Low Byte	ØØ2H	Ø1Ø2H
IOPB Address Register High Byte	ØØ3H	Ø1Ø3H
Controller Status Register (CSR)	ØØ4H	Ø1Ø4H
Controller Reset/Update Register	ØØ5H	Ø1Ø5H

Note: All addresses are in Hexadecimal.
The base I/O Port Address of Ø1ØØH is the default configuration.
The 8-bit base I/O Port Address of ØØØH is an example address.

5.4.1 iSBC® 226 BOARD I/O REGISTER ADDRESSING

The iSBC 226 board Input/Output registers are addressed as input-output byte ports on the MULTIBUS system bus. The I/O registers addresses are jumper-selectable (the default configuration is Ø1ØØH). Table 5-1 summarizes usage and addressing of the iSBC 226 board I/O registers. See Section 2.3.1 for alternate base addresses.

5.4.2 iSBC® 226 BOARD I/O REGISTER DEFINITIONS

The following sections define the iSBC 226 board I/O registers.

5.4.2.1 Relocation Registers

The relocation register is made up of two bytes. The relocation register is the most significant portion of the IOPB memory address. On power-up, this register is cleared by the iSBC 226 board. When using 16-bit addressing, this register should be zero. Writing anything except zero in this register causes IOPB relocation. See Figure 5-2 and 5-3 for an example of how 2Ø- or 24-bit addresses are determined.

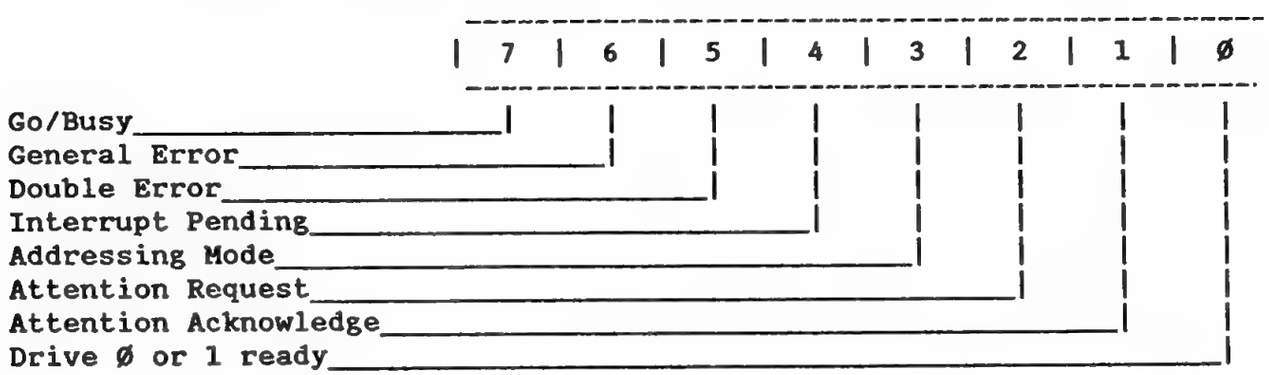
5.4.2.2 Address Registers

The address register is composed of two bytes. This register is the least significant portion of the IOPB memory address during the process of relocation. On power-up, this register is cleared by the iSBC 226 board.

5.4.2.3 Controller Status Register (CSR)

While the controller is busy, the only allowed write access to the controller registers are bits 2 and 4 of the CSR I/O port address. Any other access results in a Busy Conflict error (Ø3H).

Controller Status Register --- I/O Address ØØ4H or Ø1Ø4H



Bit	Mnemonic	Access	Meaning
7	GBSY	R/W	Go/Busy Bit - When set to one, it starts a transfer. GBSY remains set until the iSBC 226 board completes the current IOPB command or command-chain. The iSBC 226 board then clears GBSY to show readiness for another IOPB operation. While the iSBC 226 board is busy; only GBSY, IPND, and AACK are valid. When cleared, the controller is ready to perform another function.
6	ERR	R/W	General Error Bit - When set, it indicates that a hard error has been encountered and the command execution has been terminated. This bit must be cleared by an Error Reset before another command can be executed. It is set only on fatal errors. An Error Reset is accomplished by writing a one to ERR. This bit is valid only if GBSY is reset. When clear, it indicates the last IOPB did not end in a hard error.
5	DERR	R	Double Error - When set, it indicates that an error occurred and a previous error condition was not cleared. This typically means the iSBC 226 board cannot correctly write the status bytes to memory as a result of an error. A single or double error is cleared by an Error Reset or a Controller Reset. This bit is valid only if GBSY is reset. When clear, and ERR is set, a single error occurred; and STAT2 will contain the appropriate completion code. If desired, perform a Write operation using the Controller/Reset I/O Port to cause the iSBC 226 board to update the IOPB.

Controller Status Register (continued)

NOTE

It is more efficient to clear an error on the iSBC 226 board by an Error Reset (writing a one to this bit) than by using Controller Reset. Clearing by an Error Reset takes 3Ø micro-seconds, while clearing by a Controller Reset takes up to 9Ø micro-seconds.

Bit	Mnemonic	Access	Meaning
4	IPND	R/W	Interrupt Pending Bit - When set, it indicates IOPB operation is complete, the iSBC 226 board has interrupted the host CPU, and the interrupt was not serviced. The interrupt service routine clears this condition by writing a 1 to this bit before another command (except IOPB update) can be executed. This bit and the AREQ bit are the only two bits that can be written into the CSR while the iSBC 226 board is busy. This is valid all the time.

NOTE

It is more efficient to acknowledge an interrupt by an Interrupt Reset (writing a one to this bit) than by a Controller Reset. Acknowledging an interrupt by resetting the controller takes up 8Ø micro-seconds, versus approximately 3Ø micro-seconds for an Interrupt Reset.

3	ADRM	R	Addressing Mode - When set, indicates that the iSBC 226 board is jumpered for 2Ø-bit addressing mode. When this bit is set to one, it indicates the iSBC 226 board is in 24-bit addressing mode. The addressing mode is selected by a hardware jumper on the iSBC 226 board (see Section 2.3.2) and is not software selectable.

Controller Status Register (continued)

Bit	Mnemonic	Access	Meaning
2	AREQ	R/W	Attention Request - When set, it is used to gain the attention of the iSBC 226 board when it is busy processing commands. It is used in conjunction with AACK and Attention Acknowledge. Software sets AREQ and waits until the iSBC 226 board acknowledges the attention request with AACK. When AACK is set, system software may remove completed IOPBs and add new IOPBs. When work on the IOPB chain is complete, AREQ must be cleared by software. The iSBC 226 board will then clear AACK and resume operation.
1	AACK	R	Attention Acknowledge - Is set by the iSBC 226 board to acknowledge an AREQ by the system software. It is cleared by the iSBC 226 board after AREQ is cleared. If interrupt on each IOPB is enabled, an interrupt occurs when the controller sets this bit.
Ø	DRDY	R	Drive Ready - When set, it indicates the Ready-On-Cylinder status of the last drive selected. After a Controller Reset, the iSBC 226 board updates this status. When cleared, the drive is either not ready or not on cylinder.

CAUTION

System software must poll bit 0 (DRDY) in order to determine when a media change has occurred. This may be used to avoid corrupting the media structure after a removable-media section, or a disk drive, has been swapped or replaced.

5.4.2.4 Controller Reset/Update Register

Performing a Read operation using the Controller Reset/Update I/O port address causes the iSBC 226 board to perform a Controller Reset; the registers are cleared and IPND, ERR, and DERR are also cleared. The last drive selected (if none, drive Ø) is re-selected, the ready status latched, and then the drive is released. A Controller Reset does not release all dual port drives previously reserved. Reading this register causes the GBSY bit to be set while the iSBC 226 board executes the reset function.

Performing a Write operation using the Controller Reset/Update I/O port address (actual data written is insignificant) causes the iSBC 226 board to update the IOPB whose address is currently stored in the address and relocation registers. The update IOPB command writes the information contained in the iSBC 226 board internal registers back to the current IOPB. Writing this register causes the GBSY bit to set until the update is complete. An Update will update the IOPB to reflect the disk and data address at the termination of the IOPB execution. The Update also reflects any ECC error and the final sector count. On a normal termination, the sector count will be zero and the completion code will also be zero.

5.4.3 REGISTER RESPONSE

The time required to read or write registers is approximately 4ØØ nano-seconds. After any write to a register, the on-board microprocessor must update the information in its own RAM. A read or write to an iSBC 226 board register immediately after a write to a register, or a read from the Reset register, causes the iSBC 226 board to delay responding to the second transfer.

This delay, which is necessary for the microprocessor, is less than 2Ø micro-seconds for an address register write. Writing the CSR and reading or writing the Reset/update register requires up to 1ØØ micro-seconds. This delay starts after a write to any register or a read from the Reset/update register, and does not use any bus time unless another register is accessed before the delay is over. The second access will be held off only until the microprocessor has finished with the first.

5.5 INPUT/OUTPUT PARAMETER BLOCK (IOPB) DESCRIPTION

This sections covers the elements that make up an Input/Output Parameter Block (IOPB): the Command Byte, the individual bits for each Command Byte, plus their mnemonics and descriptions. See Figure 5-4 for an example of an IOPB, and Table 5-2 for definitions of the IOPB Bytes.

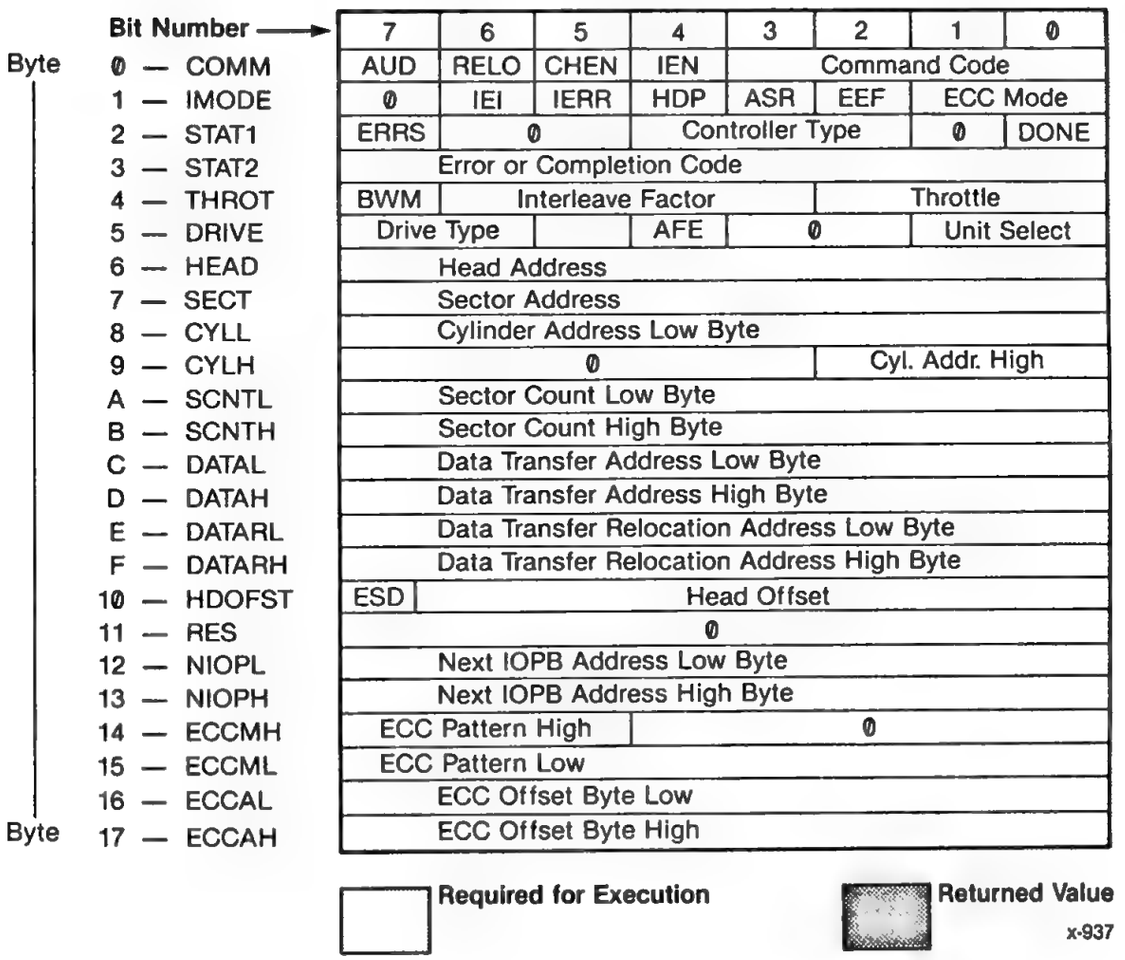


Figure 5-4. Example of an Input/Output Parameter Block (IOPB)

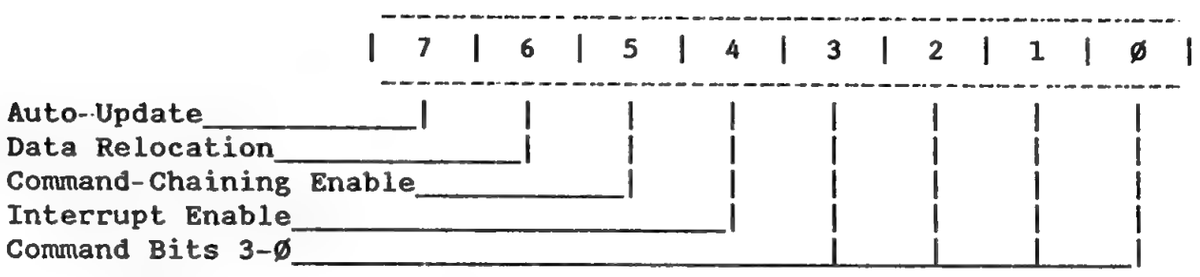
Table 5-2. iSBC® 226 Board IOPB Byte Definition

Byte Address (HEX)	Description	Mnemonic
ØØH	Disk Command	COMM
Ø1H	Interrupt Mode	IMODE
Ø2H	Status Byte 1	STAT1
Ø3H	Status Byte 2	STAT2
Ø4H	Throttle	THROT
Ø5H	Drive Type, Unit Select	DRIVE
Ø6H	Head Address	HEADH
Ø7H	Sector Address	SECT
Ø8H	Cylinder Address Low	CYLL
Ø9H	Cylinder Address High	CYLH
ØAH	Sector Count Low	SCNTL
ØBH	Sector Count High	SCNTH
ØCH	Data Address Low	DATAL
ØDH	Data Address High	DATAH
ØEH	Data Relocation Low	DATARL
ØFH	Data Relocation High	DATARH
1ØH	Head Offset	HDOFST
11H	Reserved	RES
12H	Next IOPB Address Low	NIOPs †
13H	Next IOPB Address High	HIOPH †
14H	ECC Mask Pattern High	ECCMH
15H	ECC Mask Pattern Low	ECCML
16H	ECC Bit Address Low	ECCAL
17H	ECC Bit Address High	ECCAH

Note (†): All IOPBs in a chain must be in the same 64K byte segment whose base address is specified by the iSBC 226 board IOPB Relocation Registers.

5.5.1 COMMAND BYTE (IOPB BYTE 0)

Command Byte -- (COMM)



Bit	Mnemonic	Meaning
7	AUD	Auto-Update - When set, causes the current IOPB to be updated upon its completion. The Sector, Head, Cylinder, Sector Count and Data Address bytes will reflect the result of IOPB execution.
6	RELO	Relocation - If clear, MULTIBUS data addresses are generated as 16-bit values, bits 16 through 23 are set to zero, and the Data Relocation Address bytes are ignored. If set, physical MULTIBUS addresses are formed as shown in Figure 5-2.

NOTE

This bit enables only data relocation. IOPB relocation occurs whenever the IOPB relocation registers are non-zero.

5	CHEN	Chaining Enable Bit - If clear, the iSBC 226 board executes the current IOPB and clears GBSY upon completion. If CHEN is set, the iSBC 226 board starts processing the next IOPB. The new IOPB's address is specified in the next IOPB Address bytes, and IOPB Relocation registers. The iSBC 226 board examines all chained IOPBs before initiating execution in order to optimize transfers by performing any possible overlap seek operations.
4	IEN	Interrupt Enable - If clear, the iSBC 226 board does not generate interrupts. If set, the iSBC 226 board generates an interrupt at the completion of single or chained IOPB's. If IEI and IEN are set, then an interrupt occurs at the completion of each IOPB, or when AACK is set during an Attention Request Protocol.

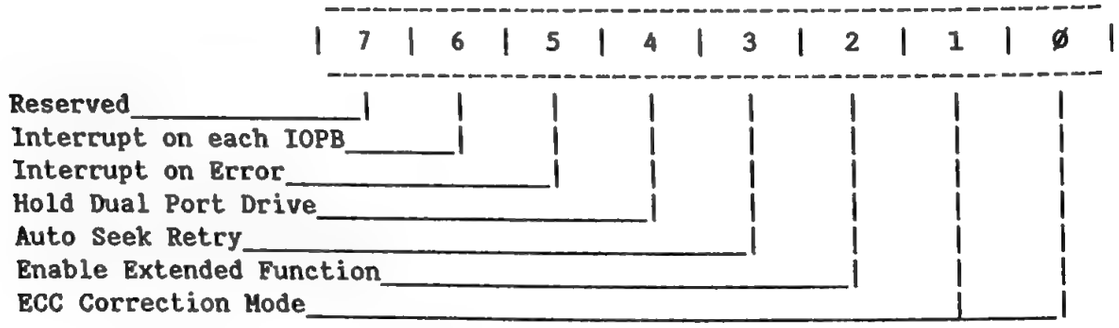
5.5.1 Command Byte (IOPB Byte 0) (continued)

Bit	Mnemonic	Meaning
3-Ø	COM	Command - Interpreted as follows:

Hex Value	Command
ØH	No Operation (NOP)
1H	Write
2H	Read
3H	Write Track Headers
4H	Read Track Headers
5H	Seek
6H	Drive Clear
7H	Write Format
8H	Read Header, Data and ECC
9H	Read Drive Status
ØAH	Write Header, Data and ECC
ØBH	Set Drive Size
ØCH	Self Test
ØDH	DMA Test
ØEH	Maintenance Buffer Load
ØFH	Maintenance Buffer Dump

5.5.2 INTERRUPT MODE/FUNCTION MODIFICATION (IOPB BYTE 1)

Interrupt Mode/Function Modification -- (IMODE)



Bit	Mnemonic	Meaning
7	----	This bit is reserved.
6	IEI	Interrupt On Each IOPB - When interrupts are enabled, and IEI is set, the iSBC 226 board interrupts each time an IOPB is completed, or when AACK is set in the CSR.
5	IERR	Interrupt On Error - This bit has no effect on the operation of the iSBC 226 board.

5.5.2 Interrupt Mode/Function Modification (IOPB Byte 1) (continued)

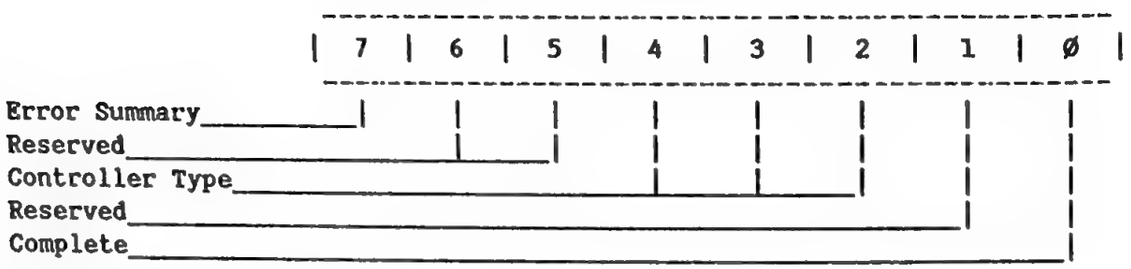
Bit	Mnemonic	Meaning
4	HDP	Hold Dual Port Drive - On a dual port drive, setting this bit prevents the iSBC 226 board from releasing the drive after the completion of the IOPB. When clear, the drive is released after each IOPB.
3	ASR	Auto Seek Retry - Enables the iSBC 226 board to re-calibrate the drive once on either a drive fault, or a Hard Seek error, and then to retry the transfer. If an auto retry was successful, a completion code of 13H is provided.
2	EEF	Enable Extended Function - When set, EEF enables commands 3 and 4, and overlapped seeking. When clear, EEF prevents the iSBC 226 board from scanning IOPBs to implement overlapped seeks.
1,Ø	ECM	ECC Correction Modes - The list below shows the four modes:

Mode	Action on Error
Ø	• Provides and ECC pattern and offset. • Stops a chained transfer (fatal error). • Reports an ECC error (1EH or Ø6H). • Loses at least one disk revolution.
1	• Does not correct or flag an error. • Continues a command chain. • Does not lose a disk revolution.
2 †	• Corrects error if possible. • Updates IOPB with soft ECC recovered error status 1FH. • Continues a command chain on soft error only. • Loses one disk revolution.
3 †	• Does not correct an error. • Flags that an error occurred (hard ECC error). • Continues a chained command. • Does not lose a disk revolution.

Note: † Soft errors that do not stop the transfer can be masked by another error. For example, in a multi-sector transfer, the second sector has an ECC recovered error, the transfer resumes and the fifth sector has a header not found error. In this case, the Header Not Found status will be written over the ECC recovered status.

5.5.3 STATUS BYTE 1 (IOPB BYTE 2)

Status Byte 1 --- (STAT1)



Bit	Mnemonic	Meaning
7	ERRS	Error Summary - When set, indicates an error occurred during IOPB processing. When clear, indicates successful completion.

NOTE

This bit does not set for soft errors or an ECC Mode 3 hard error.

6-5	---	Reserved
4-2	CTYP	Controller Type -Fixed values are shown below:

Bit 4	Bit 3	Bit 2
Ø	Ø	1

1	---	Reserved
Ø	DONE	Done - When set, this IOPB is complete and Status Byte 2 holds the completion code for the IOPB. When clear, it indicate the IOPB has not been completed.

NOTE

System software must clear (set to zero) status bytes 1 and 2 before giving the IOPB to the iSBC 226 board. If DONE is set, the iSBC 226 board will consider the IOPB complete when it reads the IOPB. Therefore, it cannot execute the IOPB.

5.5.4 STATUS BYTE 2 (IOPB BYTE 3)

When the IOPB has been executed, Status Byte 2 contains its Completion Code. Completion Codes are summarized in Table 5-3, and are described with any required corrective action in the sections that follow. Unless otherwise noted, either writing a 1 into ERR or a Controller Reset will clear a hard error. Soft errors do not stop IOPB execution.

Table 5-3. Summary of Completion Codes (IOPB Byte 3)

Code	Type	Definition
ØØH	Status	Successful Completion - No Errors
Ø1H	Hard	Interrupt Pending
Ø2H	---	Reserved
Ø3H	Hard	Busy Conflict
Ø4H	Soft	Operation Time Out
Ø5H	Hard	Header not Found
Ø6H	Hard	Hard ECC Error
Ø7H	Hard	Illegal Cylinder Address Error
Ø8H	---	Reserved
Ø9H	---	Reserved
ØAH	Hard	Illegal Sector Address
ØBH	---	Reserved
ØCH	---	Reserved
ØDH	Hard	Last Sector too Small
ØEH	Hard	Slave ACK Error (Non-existent Memory)
ØFH	---	Reserved
1ØH	---	Reserved
11H	---	Reserved
12H	Hard	Cylinder and Head Header Error
13H	Soft	Seek Retry Required
14H	Hard	Write Protect Error
15H	---	Reserved
16H	Hard	Drive Not Ready
17H	Hard	Sector Count Zero
18H	Hard	Drive Faulted
19H	Hard	Illegal Sector Size
1AH	Hard	Self Test
1BH	---	Reserved
1CH	---	Reserved
1DH	---	Reserved
1EH	Hard	Soft ECC Error
1FH	Soft	Soft ECC Error Recovered
2ØH	Hard	Illegal Head Error
21H	Hard	Disk Sequencer Error
22H	---	Reserved
24H	---	Reserved
25H	Hard	Seek Error

5.5.4.1 Completion Code Description

Code	Description
ØØH	Successful Completion - It indicates that the command is complete and that the packet may be removed from the queue.
Ø1H	Interrupt Pending Error - This error occurs when an operation is attempted with an interrupt pending. Only Interrupt Reset, Update IOPB and Controller Reset, or Error Reset operations are allowed while an interrupt is pending.
Ø2H	Reserved.
Ø3H	Busy Conflict - This error occurs if a register write is tried while GBSY is set. Bits 2 and 4 of the CSR are the only bits that can be written while the iSBC 226 board is busy.
Ø4H	Operation Timeout - The IOPB was not completed within 2 seconds. The most common problems associated with this error are: • Dual port access was not available. • The drive failed to complete a seek.
Ø5H	Header Not Found Error - This error occurs if the iSBC 226 board does not find the requested sector. Other headers were read and it was determined that the head and cylinder were correct. Some possible causes are: • The user-specified drive type and the drive type in the header do not compare. Verify and correct the drive type. • The header was found but the header ECC failed to compare. • If the drive type was correct and the error still occurs, try reformatting. If the error still occurs after reformatting, then a media defect in the header area must be assumed. The operating system should slip the sector, or log the sector bad and discontinue its use. • The actual number of sectors set in the Drive Size command exceed the specified number of sectors, plus 5. The iSBC 226 board looks for the specified number of sectors per track plus five. To determine the actual number of sectors per track and the drive type, initiate a Read Drive Status Command valid (See Section 5.6.1Ø). Example: Drive type Ø1 = 32 sectors, +5 = 37. If the drive has 47 actual sectors, there will be 1Ø sectors that may not be compared for headers. Readjust either the drive or Drive Type number of sectors per track.

5.5.4.1 Completion Code Descriptions (continued)

Code	Description
Ø6H	Hard ECC Error - This error occurs only on a Read command when the iSBC 226 board has detected a data error longer than eleven bits in the data field, or if ECC correction has been disabled (ECC Mode 3). Retry the previous Read operation. If the error still occurs, attempt to rewrite the data onto the sector in question. If the error persists, the operating system should slip the sector, or log the sector bad and discontinue its use.
Ø7H	Illegal Cylinder Address - The cylinder Address specified was greater than the maximum cylinder number allowed. Check the cylinder address and the drive parameters, then retry the operation.
Ø8H	Reserved.
Ø9H	Reserved.
ØAH	Illegal Sector Address - The Sector Address specified was greater than the maximum sector number allowed. Check the sector address and the maximum sector parameter for that drive type, then retry the IOPB operation.
ØBH	Reserved.
ØCH	Reserved.
ØDH	Last Sector Too Small - The very last sector is too small (known as a runt sector) to write a complete header. Check the drive sector switches. This error indicates a mismatch between the drive sector switches and the number of sectors per track specified by software.
ØEH	Slave ACK Error (Non-Existent Memory) - This error occurs if the memory addressed by the iSBC 226 board fails to respond. The microprocessor provides a 1Ø milli-seconds failsafe for the DMA sequencer to complete up to 128 transfers. If it does not complete them, then this error is posted. Validate the memory address or memory itself, and retry the command.
ØFH	Reserved.
1ØH	Reserved.
11H	Reserved.

5.5.4.1 Completion Code Descriptions (continued)

Code	Description
12H	Cylinder and Head Header Error - This error occurs if the cylinder or head address read from the disk fails to compare with the IOPB Cylinder and Head Address Bytes. The conditions that cause this error are: • The disk drive failed to seek to the correct cylinder. Issue a Drive Reset and retry the operation. • The disk format is corrupt. Reformat the sector in question, rewrite the data for the sector, and retry the operation. If the error persists, the operation system should slip the sector, or log the sector bad and discontinue its use. • The head byte written on the disk does not compare with the Head Address selected. This may be due to a bad format or a hardware problem.
13H	Seek Retry Required - A re-calibrate disk drive command was issued during the execution of this command to clear an error. See ASR in Section 5.5.2.
14H	Write Protect Error - This error occurs when attempting a write operation on a drive which is write-protected. Turn off write-protect and retry the write operation.
15H	Reserved.
16H	Drive Not Ready - This error occurs if the selected drive is not ready or is possibly faulted. Issue Drive Reset to the drive in question. If the drive does not become ready, check these possible causes: • Disk drive not up to operating speed or hardware error. • Bad or improperly connected A cable. • No drive of the specified Unit Number connected to the iSBC 226 board. • ACLO signal on MULTIBUS backplane connector P2 is low. • Dual port access may not have been granted.
17H	Sector Count Zero - This error is caused by issuing the iSBC 226 board an IOPB with a sector count of zero. All data Transfer operations require a positive sector count. Correct the program in error and start the transfer again.

5.5.4.1 Completion Code Descriptions (continued)

Code	Description
18H	Drive Faulted - This error code is returned when something has caused a fault in the selected disk drive. Issue Drive Reset. If the fault still exists, operator intervention is needed to correct the drive fault.
19H	Illegal Sector Size - The drive sectoring does not allow sufficient room for the header and data fields to be written. • The drive has more sector pulses, in addition to the number of specified (plus five) data sectors. • The last sector is too small to be a data sector, but has been included in the specified sector count. Adjust the drive for more sectors, or adjust the drive type for fewer sectors.
1AH	Self Test Failure - Either the microprocessor or its internal RAM failed diagnostics.
1BH	Reserved.
1CH	Reserved.
1DH	Reserved.
1EH	Soft ECC Error - This error occurs only on a Read operation when: the iSBC 226 board detects a correctable 11-bit-or-less error in the data field of the current sector, and if the ECC Mode is Ø.
1FH	Soft ECC Recovered Error - This error indicates that the ECC mode is two, and one or more ECC errors were corrected during the transfer.
2ØH	Illegal Head Address - This error occurs if the Head Address specified is greater than the maximum Head Address allowed. The maximum Head Address varies with the Drive Type specified. Correct the Drive Type and the Head Address for the drive in use, and retry the operation.
21H	Disk Sequencer Error - This error indicates that the disk sequencer did not finish its operation within the allotted time. Several things can cause this problem: • The iSBC 226 board did not receive the Servo Clock signal from the selected disk drive. A possible cause is the B cable may not be properly connected. Try a different B cable port on the iSBC 226 board.

5.5.4.1 Completion Code Descriptions (continued)

21H (continued)

- The iSBC 226 board is not receiving any read data from the selected drive. Check the B cable.
- The MULTIBUS may be preventing the iSBC 226 board from gaining proper access.

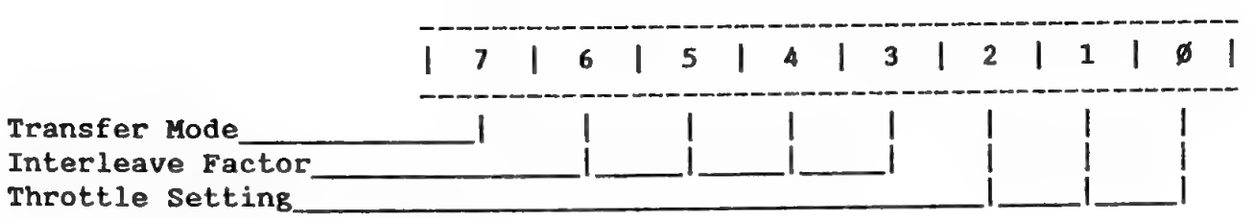
22H, 23H, 24H — Reserved.

25H — Seek Error - The drive has reported a seek error. This can be caused by selecting a cylinder higher than the drive maximum, or selecting a head beyond that supported by the drive. Check the drive parameters for the drive type you are using.

5.5.5 THROTTLE BYTE (IOPB BYTE 4)

The Throttle byte selects the number of DMA cycles in a DMA burst, word or byte mode transfers, or the Interleave Factor.

Throttle -- IOPB Byte 4



Bit	Mnemonic	Meaning
7	BWM	Transfer Mode - selects either word or byte DMA transfers between the iSBC 226 board and system memory, allowing the iSBC 226 board to operate with word- and byte-oriented memory mixtures. BWM (Byte Word Mode) should be clear when reading or writing 16-bit words in memory, or should be set when reading or writing eight-bit bytes in memory.

5.5.5 THROTTLE (IOPB BYTE 4) (continued)

6-3 --- Interleave Factor - used during format and Read/Write Header Data and ECCs. For 1:1 interleaving, the interleave factor is zero. For others the interleaving ratio is (n+1):1 where n is the interleave factor, i.e.:

Interleave Factor (Bits 6-3)	Ratio
Ø	1:1
1	2:1
2	3:1
:	:
F	16:1

NOTE

When doing interleaved formatting, always format full-track.

2-Ø THRO Throttle Setting - selects the maximum number of DMA cycles the iSBC 226 board executes each time it assumes bus mastership as shown below. During one DMA cycle, one word or one byte (depending on BWM), is transferred. This throttle value determines the DMA burst length for both data and IOPB DMA transfers.

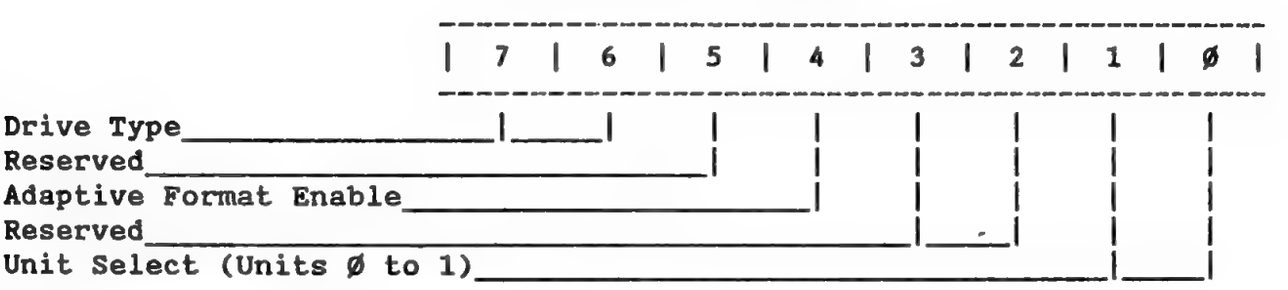
Value of Bits Ø-2	DMA Cycles
Ø	2
1	4
2	8
3	16
4	32
5	64
6	128
7	128

NOTE

Specifying a throttle value greater than 2 (eight cycles) may result in a violation of the MULTIBUS Exchange Timing Requirements. Consult the MULTIBUS Specification for more information concerning Type 1 and Type 2 equipment requirements.

5.5.6 DRIVE TYPE, UNIT SELECT (IOPB BYTE 5)

Drive Type, Unit Select



Bit	Mnemonic	Meaning
7-6	DT	Drive Type - These bits select a specific size of drive. The Drive Type bits give the software control of drives of mixed capacities, without regard to either, the iSBC 226 board B cable port they are connected to, or the logical unit number of the drive. The specific characteristics of a drive such as head offset, max head, max sector, and max cylinder are specified and defined for a specific Drive Type by a Set Drive Size command. See Section 5.6.1.
5	---	This bit is reserved.
4	AFE	Adaptive Format Enable - This bit indicates the iSBC 226 board is using Adaptive Format (i.e., the sectors are skewed). This bit is always a one.
3-2	---	These bits are reserved.
1-Ø	UNIT	The Unit Select bits contain the physical unit number of the disk unit to be accessed. Bit 1 is always a one. Bit Ø is the disk's physical unit number (either Ø or 1).

5.5.6.1 Drives with Fixed and Removable Media

Any physical drive with fixed and removable media is accessed as one logical unit (ex: the removable media or unit Ø is drive type 2, and the fixed media of unit Ø is drive type 3.) The head offset refers to the bit(s) that must be set during head tag to the drive, in order to select between the fixed and removable portions of the drive. Both the fixed and removable media are referred to by the same physical unit number. Please see Section 5.6.12.

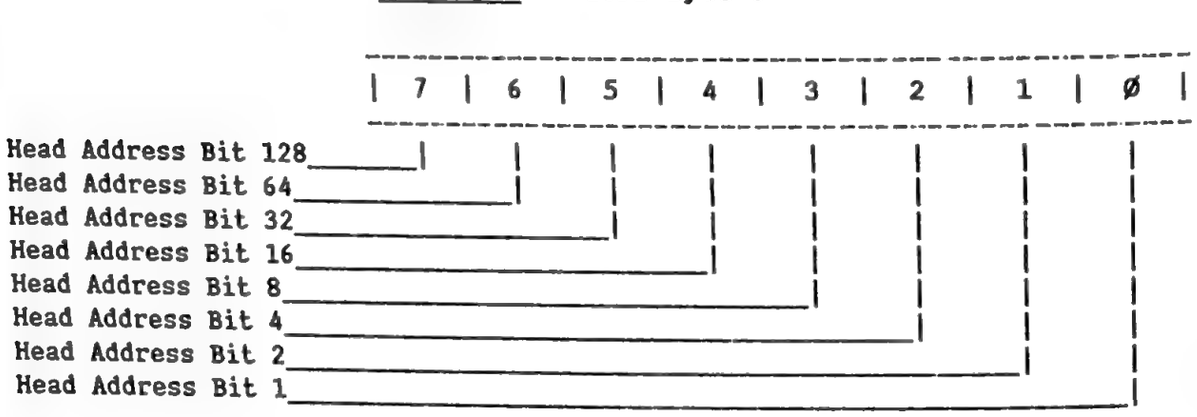
5.5.6.2 Controller Usage of Drive Type

The software must specify the Drive Type so that the iSBC 226 board will know how to address the disk drive. The Drive Type is written into the header on the disk to prevent accidental addressing of a drive with the wrong Drive Type. The Drive Type may be retrieved from a formatted disk by using a Read Header - Data - ECC command on sector zero of cylinder zero. This allows software to poll all disks to determine drive type. Consult Section 5.6.11.2 to locate the Drive Type field in the header information.

Accessing a drive with an incorrect Drive Type results in a Header Not Found Error (ØSH). It is important that the correct Drive Type be specified for the disk drive being used.

5.5.7 HEAD BYTE (IOPB BYTE 6)

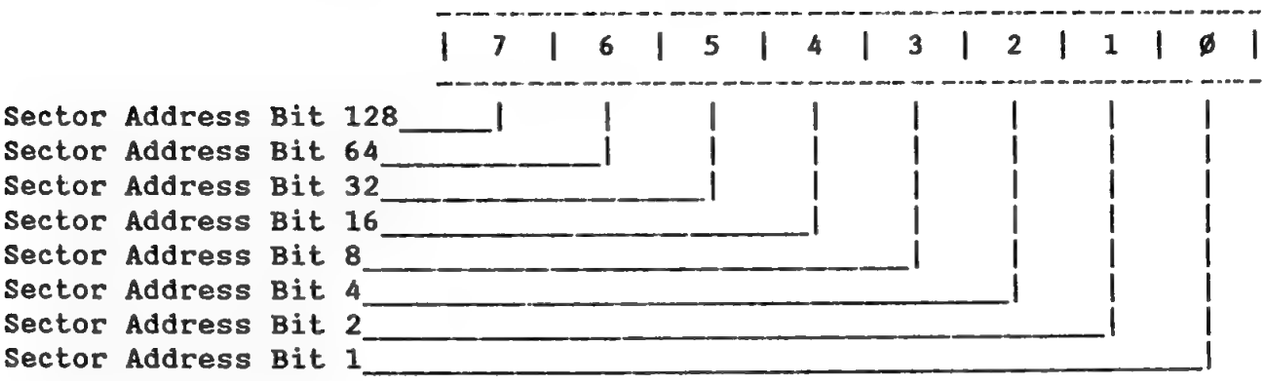
The Head Byte specifies the head number a transfer starts on. Heads are numbered starting with head Ø. Attempting to access a head number larger than max-head will cause an Illegal Head Address error.



5.5.8 SECTOR BYTE (IOPB BYTE 7)

The Sector byte specifies the starting sector number for a transfer. The sector number is used in all commands where the disk is read or written.

Sector Byte -- IOPB Byte 7



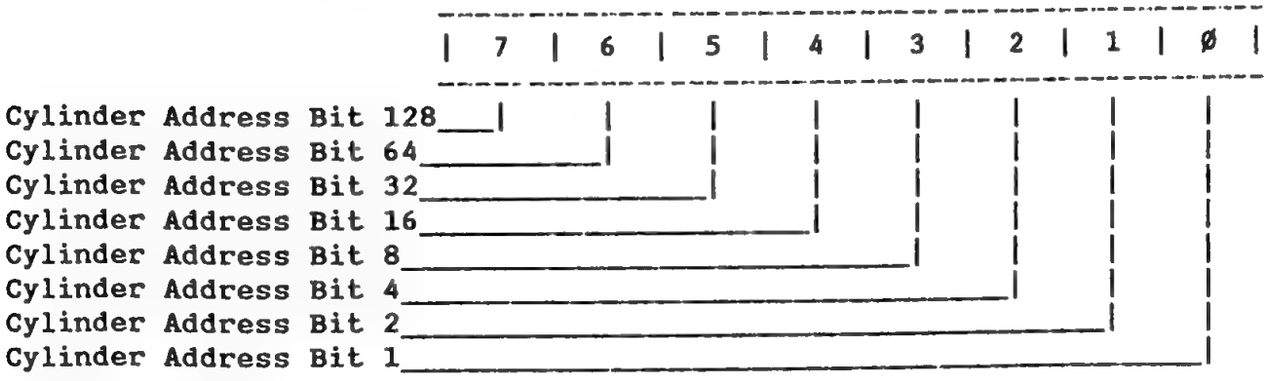
5.5.9 CYLINDER ADDRESS (IOPB BYTES 8 AND 9)

The cylinder address is specified in IOPB bytes 8 and 9. As following illustrations show, IOPB byte 8 provides the least significant 8-bits of the cylinder address and IOPB byte 9 provides the most significant 8-bits of the cylinder address. Cylinder addresses are specified in hexadecimal notation in the range of ØH through 2Ø47H.

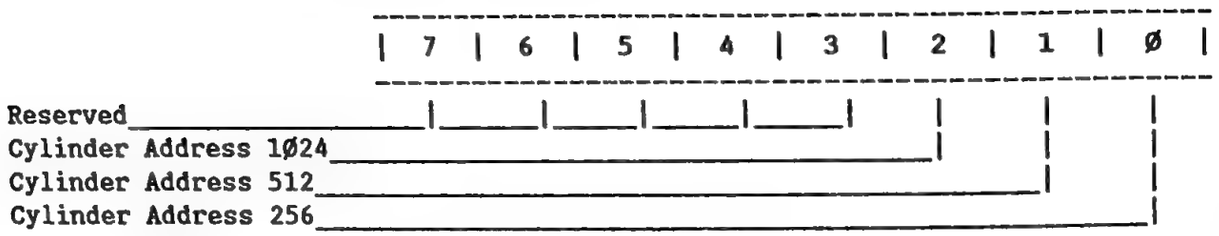
The cylinder address must be specified for all operations where data is moved to or from the disk.

As shown in the following figures, the cylinder address is an 11-bit binary number. The lower cylinder address is zero while the largest cylinder address is the number of cylinders minus 1.

Cylinder Address -- IOPB Byte 8



Cylinder Address -- IOPB Byte 9



5.5.10 SECTOR COUNT (IOPB BYTES 0AH AND 0BH)

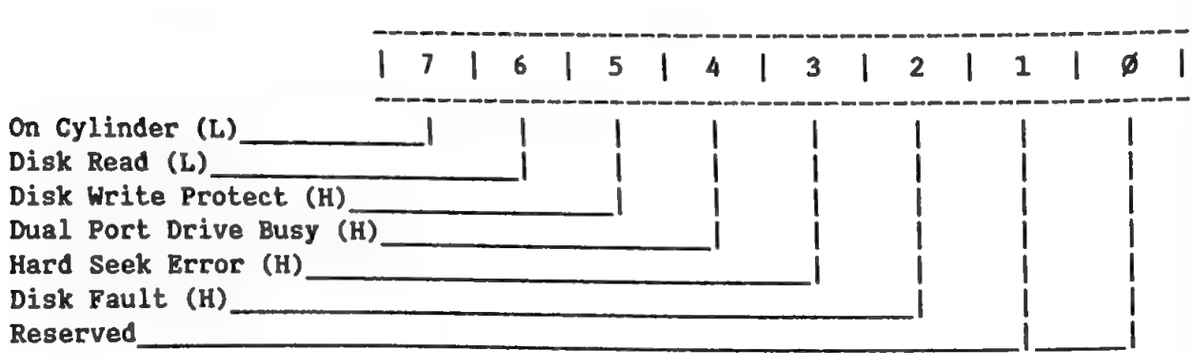
The iSBC 226 board disk controller transfers information in whole sectors. The sector count, a 16-bit number stored at two bytes in the IOPB, is the number of sectors to be transferred. Byte ØAH of the IOPB provides the least significant 8-bits of the sector count, while byte ØBH provides the most significant 8-bits. With a 16-bit sector count, execution of a continuous transfer of up to 65,535 sectors with one IOPB is possible (memory permitting).

The iSBC 226 board supports the standard sector size of 1Ø24 bytes per sector.

5.5.10.1 Sector Count (IOPB Byte 0AH) for Read Drive Status Command

On a Read Drive Status command, Byte ØAH is filled with status information from the selected drive. This is a special case in which this byte is used to return drive status information. For more detail regarding the definition of this byte, refer to Section 5.6.1Ø.

Read Drive Status Command -- IOPB Byte ØAH



Bit	Mnemonic	Meaning
7	ONCL	On Cylinder (L) - represents the On-Cylinder status of the selected drive. If the drive is ready and this bit is zero, this drive is not seeking. If this bit is a one, then the heads of the selected drive are not positioned over a cylinder.

Bit	Mnemonic	Meaning (continued)
6	DRDY	Drive Read (L) - zero if there is a drive selected and ready at this Unit Number.
5	WRPT	Disk Write Protect (H) - set when the selected disk is write protected.
4	DPB	Dual Port Busy (H) - if set, indicates that the drive is dual ported and is selected by the other controller.
3	SKER	Hard Seek Error (H) - set if the selected drive is reporting a Hard Seek Error.
2	DFLT	Disk Fault (H) - set if the selected drive is reporting any type of fault.
Ø,1	---	Reserved.

5.5.11 DATA ADDRESS (IOPB BYTES 0CH AND 0DH)

The data address is composed of two bytes. Byte ØCH is the data address low byte, and byte ØDH is the data address high byte. The data address is the memory address to, or from which, a data transfer will start.

When RELO is set, the 16-bit data address is added to a shifted Data Relocation word to form the physical starting address of a data transfer. Please see Figure 5-2.

5.5.12 DATA RELOCATION POINTER (IOPB BYTES 0EH AND 0FH)

The Data Relocation Pointer is composed of two bytes in the IOPB. Byte ØEH is the low byte and Byte ØFH is the high byte. When forming a physical address, the Data Relocation bytes and data address bytes are used to create MULTIBUS addresses, as shown in Figure 5-2. However, the Data Relocation bytes are ignored if RELO is clear in the IOPB Command Byte.

5.5.13 HEAD OFFSET AND DRIVE SERVO TYPE (IOPB BYTE 10H)

The Head Offset byte is used by the Set Drive Size and Read Drive Status commands. It determines the offset required to access a fixed or removable section of a fixed/removable drive. The selection of fixed or removable media, is done by specifying the head that addressed that section. Typically, the heads are separated into numerical groups, ex: heads ØXH are removable media, and heads 1XH are fixed media (where X is the relative head address for that media). This byte contains the bits which must be added to the head value, which is sent to the drive to

select either the fixed or removable portion of the drive. For example, in the case of a Cartridge Module Drive; the Head Offset must equal 1ØH when defining the fixed portion of the drive, and Ø for the removable portion. In both cases, the drive unit number will be Ø for Drive Ø.

When bit 7 of byte 1ØH is set, software selects a seek after every head change, which is required when using an embedded servo disk drive. This seek is required by the drive in order to lock onto the new track. When using an embedded servo drive, the drive should be configured for the mode that requires the controller to issue a seek on each head change. However, it may not be required to set this bit on embedded servo drives that provide this feature automatically. See Section 5.6.12.5 for further detail.

5.5.14 RESERVED (IOPB BYTE 11H)

This Byte is reserved.

5.5.15 NEXT IOPB ADDRESS (IOPB BYTES 12H AND 13H)

When using command chaining, the starting address of the next IOPB must be specified. These two bytes (bytes 12H and 13H) are combined with the IOPB Relocation registers to determine the next IOPB address. They are the missing link in the IOPB chain.

Byte 12H is the low byte and byte 13H is the high byte of the Next IOPB Address. These two bytes make up a 16-bit address similar to the IOPB Address Register. The Next IOPB Address is added to the IOPB Relocation Register to form a physical address (Figure 5-2). This physical address is 1Ø- or 24-bits in length, depending on the addressing mode selected and is used as the pointer to the next IOPB in the chain. All IOPBs in a chain are relative to the same relocation address, and thus must be within a 64K byte block of memory.

To enable command chaining, set CHEN in the Command byte of the IOPB. If command chaining is not enabled, bytes 12H and 13H are ignored.

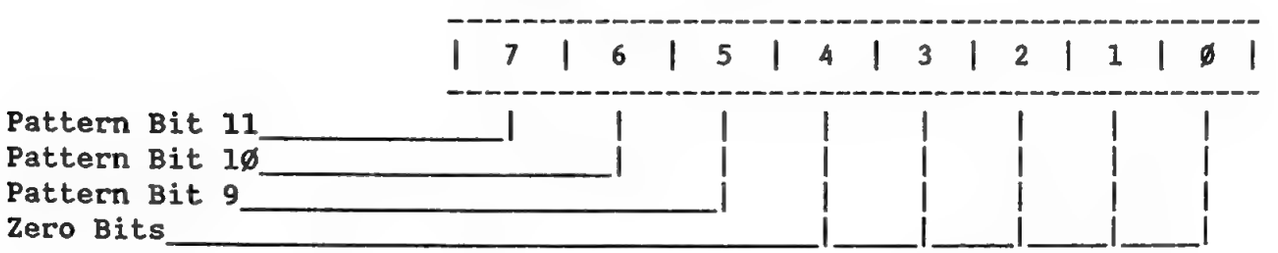
5.5.16 ECC PATTERN WORD (IOPB BYTES 14H AND 15H)

The ECC Pattern or Mask Word is a 11-bit word used in the soft ECC correction procedure. The ECC Pattern Word is stored in IOPB Bytes 14H and 15H. A Soft ECC Error is defined as any single error of 11 bits or less. The error is still considered soft if there are incorrect bits at each end of the an 11-bit word, but the bits in the center are correct. This word provides a pattern to correct data in memory.

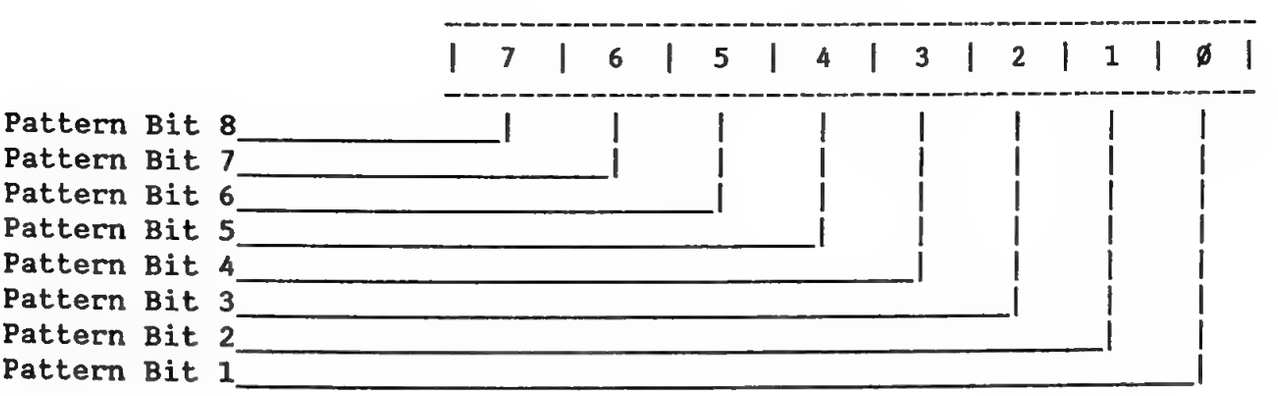
5.5.16 ECC PATTERN WORD (IOPB BYTES 14H AND 15H) (continued)

The ECC Pattern Word is calculated by the iSBC 226 board and left in reverse order, in IOPB Bytes 14H and 15H as illustrated below. Before using the ECC Pattern Word, a bit-reversal process must be executed to correct the direction of this mask, in relation to the data stream it will correct. After the reversal process, the equivalent word will have Pattern Bit Ø in Bit 16, Pattern Bit 1 in Bit 15, and so on. The five least-significant bits will be zero. See Section 5.6.3.7.

ECC Pattern Byte 14H



ECC Pattern Byte 15H



5.5.17 ECC ADDRESS WORD (IOPB BYTES 16H AND 17H)

When a Soft ECC Error occurs, the iSBC 226 board also calculates an ECC Address Word. Two bytes are used to store the ECC Address Word. IOPB byte 17H is the most significant, and IOPB byte 16H is the least significant. This address word points to the bit within a sector where the data in error states. By EXclusive ORing the ECC mask with this bit string, the error may be corrected.

5.6 COMMANDS

The four least-significant bits of the Command byte are the IOPB Command bits. These four bits allow up to sixteen possible commands, one of which is reserved. Each command will start at the beginning of a page, will have a short description, and a reference IOPB. The IOPBs are encoded to show which bytes are required for execution, and which are returned after execution. The bytes indicated are returned with or without an update.

The commands are transferred to the iSBC 226 board via a 24-byte long IOPB. Each iSBC 226 board command requires different IOPB bytes. In general, all commands use bytes ØH thru ØFH, with bytes 1ØH through 17H being dependant on the command executed. Only the Read command uses ECC bytes 14H through 17H. Although all bytes must be reserved, most commands do not use the entire IOPB.

5.6.1 NOP COMMAND (COMMAND CODE 0)

The No Operation (NOP) command causes the controller to select a disk drive, save DRDY (bit Ø of CSR), and release the drive.

5.6.1.1 IOPB

NOP

Byte		Bit 7	6	5	4	3	2	1	0
0	COMM	AUD	RELO	CHEN	IEN	Command Code			
1	IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
2	STAT1	ERRS	0		Controller Type			0	DONE
3	STAT2	Error or Completion Code							
4	THROT	BWM	Interleave Factor				Throttle		
5	DRIVE	Drive Type			AFE	0		Unit Select	
6	HEAD	Head Address							
7	SECT	Sector Address							
8	CYLL	Cylinder Address Low Byte							
9	CYLH	0					Cyl. Addr. High		
A	SCNTL	Sector Count Low Byte							
B	SCNTH	Sector Count High Byte							
C	DATAL	Data Transfer Address Low Byte							
D	DATAH	Data Transfer Address High Byte							
E	DATARL	Data Transfer Relocation Address Low Byte							
F	DATARH	Data Transfer Relocation Address High Byte							
10	HDOFST	ESD	Head Offset						
11	RES	0							
12	NIOPL	Next IOPB Address Low Byte							
13	NIOPH	Next IOPB Address High Byte							
14	ECCMH	ECC Pattern High	0						
15	ECCML	ECC Pattern Low							
16	ECCAL	ECC Offset Byte Low							
17	ECCAH	ECC Offset Byte High							

Required for Execution

Returned Value

x-911

5.6.2 WRITE COMMAND (COMMAND CODE 1)

The Write command transfers data to the disk. It starts at the disk and memory addresses specified in the IOPB, and transfers as many sectors as requested. The iSBC 226 board crosses cylinder, head, and sector boundaries as required.

5.6.2.1 IOPB

WRITE

Byte	Bit Number →	7	6	5	4	3	2	1	0
	0 — COMM	AUD	RELO	CHEN	IEN	Command Code			
	1 — IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
	2 — STAT1	ERNS	0		Controller Type			0	DONE
	3 — STAT2	Error or Completion Code							
	4 — THROT	BWM	Interleave Factor				Throttle		
	5 — DRIVE	Drive Type			AFE	0		Unit Select	
	6 — HEAD	Head Address							
	7 — SECT	Sector Address							
	8 — CYLL	Cylinder Address Low Byte							
	9 — CYLH	0					Cyl. Addr. High		
	A — SCNTL	Sector Count Low Byte							
	B — SCNTH	Sector Count High Byte							
	C — DATAL	Data Transfer Address Low Byte							
	D — DATAH	Data Transfer Address High Byte							
	E — DATARL	Data Transfer Relocation Address Low Byte							
	F — DATARH	Data Transfer Relocation Address High Byte							
	10 — HDOFST	ESD	Head Offset						
	11 — RES	0							
	12 — NIOPL	Next IOPB Address Low Byte							
	13 — NIOPH	Next IOPB Address High Byte							
	14 — ECCMH	ECC Pattern High	0						
	15 — ECCML	ECC Pattern Low							
	16 — ECCAL	ECC Offset Byte Low							
Byte	17 — ECCAH	ECC Offset Byte High							

Required for Execution Returned Value

x-912

5.6.2.2 Implied Seeks

The iSBC 226 board issues an implied seek on a Write command. This seek will be issued as the first operation after reading the IOPB from system memory. If chained operations are implemented, the EEF bit is set, and the iSBC 226 board will scan the remainder of the chain for the possibility of overlap seeks.

5.6.2.3 Filling Buffer

When the seek is complete, the iSBC 226 board accesses the IOPB to determine the command parameters, and begins to fill the FIFO buffer. After sufficient data (minimum of one sector) is in the buffer, the controller begins to look for sector coincidence. This process ensures that sufficient data is available in the buffer at the start of the write.

5.6.2.4 Sector Coincidence

The iSBC 226 board selects the proper head and tests the write protect status of the drive. The iSBC 226 board will then read each sector header and compare it to the requested disk address. When a match is found, the data transfer begins. If a match is not found within one revolution plus five sectors, an error of 5H or 12H will be generated.

5.6.2.5 Write Data

After a valid header has been found, the disk sequencer will count the appropriate number of bytes and then write the sync bits. It will then take words out of the FIFO, serialize them, generate a new ECC value, and write them to the disk. As data is removed from the FIFO, data is replaced through a new DMA cycle from system memory.

5.6.2.6 Throttle

The throttle is the maximum number of transfers that are allowed each time the iSBC 226 board becomes bus master. On a write operation, the first DMA bursts will be at the programmed throttle value until the buffer is full. After data starts moving to the disk, the typical burst will be less than the throttle value. Words will continue to be transferred into the FIFO buffer as required until the sector count goes to zero.

5.6.2.7 ECC

After the data field of a sector has been written, the ECC value generated from the data field is written.

5.6.2.8 Incrementing Disk Address

The sector address increments by 1 as each sector is written. If the sector address is greater than max sector, the sector is reset to zero and the head address is incremented. If the resultant head address is greater than maximum head, the head address is reset to zero and the cylinder address will then be incremented by one. If the cylinder address is greater than maximum cylinder when the implied seek is issued, an error is generated.

5.6.2.9 Completing a Transfer

The sector count is decremented by 1 for each sector transferred. At the end of the sector, the sector count is tested to determine if the transfer is complete. If the transfer is not complete, the next sector is transferred. If the cylinder address had been incremented to a legal address, an implied seek is issued.

When the transfer is complete, the two status bytes of the IOPB are updated and if interrupts are enabled, an interrupt is generated. If AUD of the IOPB command byte was set, the IOPB will be updated.

If the transfer ends in a hard error; the transfer is stopped, the two status bytes of the IOPB are updated; and if interrupts are enabled, an interrupt is generated. Any chained operations will be halted. The IOPB address and relocation registers will be pointing to the IOPB which caused the error. If AUD was set, the IOPB will be updated.

A Header Not Found occurs during a Write if the iSBC 226 board encounters a sector previously marked bad (not slipped) by a Write HDE command. If AUD is set, the remaining number of sectors not written posts in the Sector Count field, and the sector in error posts in the Sector Address field. This allows you to individually map bad sectors via software and also receive status information enabling you to restart the transfer at the correct sector.

If the transfer ends with a soft error; the two status bytes of the IOPB are updated, and if interrupts are enabled, an interrupt is generated. Any chained operations will be continued. If AUD was set, the IOPB will be updated. The ERR bit of the CSR will not be set since this is a soft error.

5.6.3 READ COMMAND (COMMAND CODE 2)

The Read Command transfers data from the disk to memory. The command will transfer data from the disk to memory, starting at the disk and memory addresses specified in the IOPB; and cross sector, head, and cylinder boundaries as required.

5.6.3.1 IOPB

READ

Byte	Bit Number →	7	6	5	4	3	2	1	0
0	0 — COMM	AUD	RELO	CHEN	IEN	Command Code			
1	1 — IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
2	2 — STAT1	ERRS	0		Controller Type			0	DONE
3	3 — STAT2	Error or Completion Code							
4	4 — THROT	BWM	Interleave Factor				Throttle		
5	5 — DRIVE	Drive Type			AFE	0		Unit Select	
6	6 — HEAD	Head Address							
7	7 — SECT	Sector Address							
8	8 — CYLL	Cylinder Address Low Byte							
9	9 — CYLH	0					Cyl. Addr. High		
A	A — SCNTL	Sector Count Low Byte							
B	B — SCNTH	Sector Count High Byte							
C	C — DATAL	Data Transfer Address Low Byte							
D	D — DATAH	Data Transfer Address High Byte							
E	E — DATARL	Data Transfer Relocation Address Low Byte							
F	F — DATARH	Data Transfer Relocation Address High Byte							
10	10 — HDOFST	ESD	Head Offset						
11	11 — RES	0							
12	12 — NIOPL	Next IOPB Address Low Byte							
13	13 — NIOPH	Next IOPB Address High Byte							
14	14 — ECCMH	ECC Pattern High				0			
15	15 — ECCML	ECC Pattern Low							
16	16 — ECCAL	ECC Offset Byte Low							
17	17 — ECCAH	ECC Offset Byte High							

Byte

Required for Execution

Returned Value

x-913

5.6.3.2 Implied Seeks

The iSBC 226 board will issue an implied seek on a Read command. This seek will be issued as the first operation after reading the IOPB from system memory. If chained operations are implemented, and the EEF bit is set, the iSBC 226 board will scan the remainder of the chain for the possibility of overlap seeks.

5.6.3.3 Seek End

The iSBC 226 board scans the drives to determine when a drive has completed its seek.

5.6.3.4 Sector Coincidence

The iSBC 226 board reads each sector header and compares it to the requested disk address. When a comparison is true, the transfer process is initiated. If a comparison is not true within one revolution, plus five sectors, the appropriate error is generated.

5.6.3.5 Read Data

After a valid header match, the disk sequencer waits for the sync bits for the data field. As data is read in from the disk it is de-serialized and placed into the FIFO buffer. When data becomes available at the other end of the FIFO, the iSBC 226 board requests the bus and transfers the data to memory via DMA. The serial stream of data is also used to generate an ECC.

5.6.3.6 Throttle

The throttle is the maximum number of transfers that are allowed each time the iSBC 226 board becomes a bus master. On a read operation, the first DMA bursts will be at minimum value. This is because the limiting factor of the DMA burst length is the number of words available from the FIFO. After the initial few DMA bursts, the typical burst length will increase, possibly approaching the throttle limit. Words will continue to be transferred from the controller as required until the sector count goes to zero and the buffer is empty.

5.6.3.7 ECC

When the data field of a sector has been read, the ECC value generated by the iSBC 226 board during the read is compared to the ECC written on the disk during the original write.

5.6.3.8 Incrementing Disk Address

The sector address increments by 1 as each sector is read. If the sector address is greater than max sector, it resets to zero and the head address is incremented. If the resultant head address is greater than maximum head, then the head address is reset to zero and the cylinder address is incremented by one. If the cylinder address is greater than maximum cylinder when the implied seek is issued, an error is generated.

5.6.3.9 Completing a Transfer

At the end of the sector, the sector count is tested to determine if the transfer is complete. If the transfer is not complete, the next sector is transferred. If the cylinder address has just been incremented to a legal value, an implied seek is issued.

When the transfer is complete, the two status bytes of the IOPB are updated, and if interrupts are enabled, an interrupt is generated. If AUD of the IOPB command byte was set, the IOPB is then updated.

If the transfer ends in a hard error; the transfer is stopped, the two status bytes of the IOPB are updated; and if any interrupts are enabled, an interrupt is generated. Any chained operations are halted. The IOPB address and relocation registers will then be pointing to the IOPB which caused the error. If AUD was set, the IOPB is updated.

A Header Not Found occurs during a Read if the iSBC 226 board encounters a sector previously marked bad (not slipped) by a Write HDE command. If AUD is set, the remaining number of sectors not read posts in the Sector Count field, and the sector in error posts in the Sector Address field. This allows you to individually map bad sectors via software and also receive status information enabling you to restart the transfer at the correct sector.

If the transfer ends with a soft error, the two status bytes of the IOPB are updated; and if interrupts are enabled, an interrupt is generated. Any chained operations are continued. If AUD was set, the IOPB is updated. The ERR bits in the CSR and STAT 1 do not set on a soft error.

5.6.3.10 Read Command Encounters an ECC Error in ECC Mode 0

When the ECC value calculated from a Read does not compare with the ECC value written on the disk, the iSBC 226 board stops reading. All data for that sector is written to memory and an ECC calculation begins. Through a shifting and counting process, the iSBC 226 board determines where and how much of an error occurred.

If the iSBC 226 board encounters an error larger than 11 bits (hard error), it writes the Error Code Ø6H into the Completion Code Byte.

If the iSBC 226 board encounters an error of 11 bits or less (soft error), it writes the ECC Pattern and Address Words to their IOPB bytes, and issues Error Code 1E.

When the iSBC 226 board encounters an ECC Error, the internal registers are in the following state: the disk address points to the sector containing the error; the Data Address and Relocation address points to the first byte of data from the sector following the sector in error; and, the sector count is equal to the number of sectors remaining, plus 1. To retrieve this information, either set AUD or issue a write to the Update IOPB register. This identifies the offending sector and its related Data Address.

To continue the transfer after a soft error, update the sector count (subtract 1), update the disk address, and then restart the IOPB.

5.6.3.11 Read Command Encounters an ECC Error in Mode 1

ECC errors are not detected in this mode. The data transfer continues because no error was encountered.

5.6.3.12 Read Command Encounters an ECC Error in Mode 2

If an ECC correctable error is encountered in Mode 2, the iSBC 226 board stops the transfer, corrects the data in memory, and resumes transferring data on the next revolution of the disk. A soft ECC recovered error will be reported in the IOPB, and if chain mode is enabled, the command chain continues. The iSBC 226 board performs corrections in byte wide DMA transfers.

5.6.3.13 Read Command Encounters an ECC Error in Mode 3

If the iSBC 226 board detects an ECC error, the data transfer continues as if no error was detected. When the transfer completes, the error status code in the IOPB displays the Hard ECC error code of Ø6H. This indicates that one or more uncorrected ECC errors were encountered. This error reports as "soft", as it does not stop a chain. ERR and ERS do not set on this error in Mode 3.

5.6.4 WRITE TRACK HEADERS (COMMAND CODE 3)

The Write Track Header command and Read Track Headers provide the ability to avoid media defects by slipping sectors. The Write Track Headers command formats an entire track with header data which is resident in system memory. The Read Track Headers command transfers the header data into system memory. This data is the actual header for each sector on the track starting at pseudo index, including bad and spare sectors. As this is a format command, all data on that track is overwritten (see Section 5.7.4). This command only functions when enabled by setting the EFF bit.

5.6.4.1 IOPB

WRITE TRACK HEADERS

Byte	7	6	5	4	3	2	1	0
0 — COMM	AUD	RELO	CHEN	IEN	Command Code			
1 — IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
2 — STAT1	ERRS	0		Controller Type			0	DONE
3 — STAT2	Error or Completion Code							
4 — THROT	BWM	Interleave Factor				Throttle		
5 — DRIVE	Drive Type			AFE	0		Unit Select	
6 — HEAD	Head Address							
7 — SECT	Sector Address							
8 — CYLL	Cylinder Address Low Byte							
9 — CYLH	0					Cyl. Addr. High		
A — SCNTL	Sector Count Low Byte							
B — SCNTH	Sector Count High Byte							
C — DATAL	Data Transfer Address Low Byte							
D — DATAH	Data Transfer Address High Byte							
E — DATARL	Data Transfer Relocation Address Low Byte							
F — DATARH	Data Transfer Relocation Address High Byte							
10 — HDOFST	ESD	Head Offset						
11 — RES	0							
12 — NIOPL	Next IOPB Address Low Byte							
13 — NIOPH	Next IOPB Address High Byte							
14 — ECCMH	ECC Pattern High	0						
15 — ECCML	ECC Pattern Low							
16 — ECCAL	ECC Offset Byte Low							
17 — ECCAH	ECC Offset Byte High							

Bit Number →

Required for Execution

Returned Value

x-915

NOTE

System software must specify a non-zero count when using this command.

5.6.4.2 Data Buffer

A data buffer must be constructed in system memory prior to issuing a Write Track Headers command. The Read Track Headers command will construct a proper buffer in host memory. This buffer consists of four bytes of data for each sector; therefore, the total buffer length is four bytes times the total number of sectors on the track (including spare and bad sectors). The iSBC 226 board counts the actual number of sectors on the drive. This count is used as the number of sectors for the Write Track Headers command. The first four bytes will be the header data for sector zero, the first sector after pseudo index. The next four bytes are for the next sector, etc.

5.6.4.3 Implied Seeks

The iSBC 226 board issues an implied seek on a Write Track Headers command. The seek is issued as the first operation after reading the IOPB from system memory. If chained operations are implemented, and the EEF bit is set, the iSBC 226 board scans the remainder of the chain for the possibility of overlap seeks.

5.6.4.4 Seek End

The iSBC 226 board scans the drives to determine when a drive has completed its seek. When the requested drive has completed its seek, the iSBC 226 board accesses the IOPB to determine the command parameters, and then begins to fill its buffer. When sufficient data is in the buffer, the search for pseudo index will begin.

5.6.4.5 Throttle

The Throttle is the maximum number of DMA transfers that can occur each time the iSBC 226 board becomes the bus master. On a Write Track Headers operation the DMA bursts will be at the specified throttle. The DMA transfers will continue until enough data is available to format an entire track.

5.6.4.6 Pseudo Index

The pseudo index is delayed from the physical index by one sector per track in the iSBC 226 board adaptive format. When the index has arrived under the head, the first four bytes of data are used to format that sector. The iSBC 226 board automatically calculates and appends the ECC to the header.

5.6.4.7 Format the Track

As each successive sector arrives under the head, four bytes are taken from the buffer and used as the header for that sector. The data field portion of the sector is not written by a Write Track Headers command. Therefore, the data is invalid after this operation. This operation continues for each sector on the requested track.

5.6.4.8 Incrementing Disk Address

The sector address is incremented by 1 for each sector written. At the end of a successful command the head address is incremented by 1. If the resultant head address is greater than maximum head, it is cleared and the cylinder address is incremented.

5.6.4.9 Completing a Transfer

The iSBC 226 board formats the headers of an entire track if errors are not encountered. When the format is complete, the two status bytes are updated. If AUD is set, the IOPB is updated, and if interrupts are enabled, an interrupt is generated.

If the transfer ends in a hard error, the transfer is stopped and any chained operations are also terminated. The two status bytes are then updated. If AUD is set, the IOPB is updated, and if interrupts are enabled, an interrupt is generated.

If the transfer ends in a soft error, the transfer has completed, and chained operations are not terminated. The two status bytes are updated, if AUD is set, the IOPB will be updated; and if interrupts are enabled, an interrupt is generated.

5.6.4.10 Marking an Entire Track Bad

If several sectors on a track are known bad, it is desirable in certain applications to label the entire track bad, and then map the track bad via software. In order to mark the entire track bad, a 7FH pattern must be written in the four header bytes.

5.6.5 READ TRACK HEADERS (COMMAND CODE 4)

The Read Track Headers command and Write Track Headers provide the ability to avoid media defects by slipping sectors. The Read Track Headers command reads the header from each physical sector starting at pseudo index and transfers the data in order to system memory. The headers may not be in sequential order due to interleaving and sector slip. The Write Track Headers command writes the headers back to the track. The buffer contains the actual header data from each sector on the track starting at pseudo index, including bad and spare sectors. The sector count field must be non-zero for this command. This command functions only if enabled by setting the EFF bit.

5.6.5.1 IOPB

READ TRACK HEADERS

	Bit Number →	7	6	5	4	3	2	1	0
Byte	0 — COMM	AUD	RELO	CHEN	IEN	Command Code			
	1 — IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
	2 — STAT1	ERRS	0		Controller Type			0	DONE
	3 — STAT2	Error or Completion Code							
	4 — THROT	BWM	Interleave Factor				Throttle		
	5 — DRIVE	Drive Type			AFE	0		Unit Select	
	6 — HEAD	Head Address							
	7 — SECT	Sector Address							
	8 — CYLL	Cylinder Address Low Byte							
	9 — CYLH	0					Cyl. Addr. High		
	A — SCNTL	Sector Count Low Byte							
	B — SCNTH	Sector Count High Byte							
	C — DATAL	Data Transfer Address Low Byte							
	D — DATAH	Data Transfer Address High Byte							
	E — DATARL	Data Transfer Relocation Address Low Byte							
	F — DATARH	Data Transfer Relocation Address High Byte							
	10 — HDOFST	ESD	Head Offset						
	11 — RES	0							
	12 — NIOPL	Next IOPB Address Low Byte							
	13 — NIOPH	Next IOPB Address High Byte							
	14 — ECCMH	ECC Pattern High				0			
	15 — ECCML	ECC Pattern Low							
	16 — ECCAL	ECC Offset Byte Low							
Byte	17 — ECCAH	ECC Offset Byte High							

Required for Execution Returned Value

x-914

NOTE

System software must specify a non-zero count when using this command.

5.6.5.2 Data Buffer

A data buffer must be allocated in system memory prior to issuing a Read Track Headers command. The total buffer length should be four bytes times the total number of sectors on the track (including spare and bad sectors). The iSBC 226 board counts the actual number of sectors on the drive. This count is used as the number of sectors for the Read Track Headers command.

5.6.5.3 Implied Seeks

The iSBC 226 board issues an implied seek on a Read Track Headers command. The seek is issued as the first operation after reading the IOPB from system memory. If chained operations are implemented, and the EEF bit is set, the iSBC 226 board scans the remainder of the chain for the possibility of overlap seeks.

5.6.5.4 Seek End

The iSBC 226 board scans the drives to determine when the drive has completed its seek. When the requested drive has completed its seek, the iSBC 226 board accesses the IOPB to determine the command parameters and initiates a search for pseudo index.

5.6.5.5 Pseudo Index Versus Physical Index

Pseudo index is delayed from physical index by one sector per track in the iSBC 226 board adaptive format. When the physical index has arrived under the head, the first four bytes of data are used to format that sector. The iSBC 226 board automatically calculates and appends the ECC to the header.

5.6.5.6 Read the Track

As each sector arrives under the head, four bytes are read from the header and transferred to the buffer. This operation continues for each sector on the requested track.

5.6.5.7 Empty Buffer

When a complete track has been read, the iSBC 226 board writes the header data directly to system memory.

5.6.5.8 Throttle

The throttle is the maximum number of DMA transfers that can occur each time the iSBC 226 board becomes the bus master. On a Read Track Headers operation, the DMA bursts are at the specified throttle value. The DMA transfers continue until all data has been transferred to system memory.

5.6.5.9 Incrementing Disk Address

The sector address is incremented by 1 for each sector read. At the end of a successful command the head address is incremented by 1. If the resultant head address is greater than maximum head, it is cleared and the cylinder address is incremented.

5.6.5.10 Completing a Transfer

If the iSBC 226 board encounters no errors, it Reads the headers of an entire track. When the transfer is completed, it updates the two status bytes; and if interrupts are enabled, generates an interrupt. If AUD is set, the iSBC 226 board updates the IOPB.

The iSBC 226 board stops a transfer that ends in a hard error, terminates any chained operations, and updates the two status bytes; if interrupts are enabled, the iSBC 226 board also generates an interrupt. If AUD is set, the iSBC 226 board updates the IOPB.

The iSBC 226 board completes a transfer that ends in a soft error, continues any chained operations, and updates the two status bytes; if interrupts are enabled, the iSBC 226 board also generates an interrupt. If AUD is set, the iSBC 226 board updates the IOPB.

5.6.6 SEEK (COMMAND CODE 5)

The Seek command moves the heads of the selected disk drive to the address specified in the IOPB Cylinder Address. This command is used mainly for diagnostic purposes because an Implied Seek is inherent in data transfer commands. The iSBC 226 board may initiate overlapped seeking when IOPBs for different drives are chained together by software.

5.6.6.1 IOPB

SEEK

Byte	Bit Number →	7	6	5	4	3	2	1	0
	0 — COMM	AUD	RELO	CHEN	IEN	Command Code			
	1 — IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
	2 — STAT1	CRCS	0		Controller Type			0	CONE
	3 — STAT2	Error or Completion Code							
	4 — THROT	BWM	Interleave Factor				Throttle		
	5 — DRIVE	Drive Type			AFE	0		Unit Select	
	6 — HEAD	Head Address							
	7 — SECT	Sector Address							
	8 — CYLL	Cylinder Address Low Byte							
	9 — CYLH	0					Cyl. Addr. High		
	A — SCNTL	Sector Count Low Byte							
	B — SCNTH	Sector Count High Byte							
	C — DATAL	Data Transfer Address Low Byte							
	D — DATAH	Data Transfer Address High Byte							
	E — DATARL	Data Transfer Relocation Address Low Byte							
	F — DATARH	Data Transfer Relocation Address High Byte							
	10 — HDOFST	ESD	Head Offset						
	11 — RES	0							
	12 — NIOPL	Next IOPB Address Low Byte							
	13 — NIOPH	Next IOPB Address High Byte							
	14 — ECCMH	ECC Pattern High	0						
	15 — ECCML	ECC Pattern Low							
	16 — ECCAL	ECC Offset Byte Low							
Byte	17 — ECCAH	ECC Offset Byte High							

Required for Execution Returned Value

x-916

5.6.6.2 Detailed Description of Seek (Command Code 5)

A Seek command starts the appropriate seek by sending the cylinder address to the disk drive. The iSBC 226 board scans the drives to determine when each drive completes its seek. After the Seek completes, the iSBC 226 board marks the associated IOPB as completed. Explicit Seek commands overlap if the EEF bit is set (like Implied Seeks).

5.6.7 DRIVE CLEAR (COMMAND CODE 6)

The Drive Clear command clears a Drive Fault and returns the drive to Cylinder Zero (Return to Zero or Re-calibrate).

5.6.7.1 IOPB

DRIVE RESET

Byte		Bit Number → 7	6	5	4	3	2	1	0
	0 — COMM	AUD	RELO	CHEN	IEN	Command Code			
	1 — IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
	2 — STAT1	ERRS	0		Controller Type			0	DONE
	3 — STAT2	Error or Completion Code							
	4 — THROT	BWM	Interleave Factor				Throttle		
	5 — DRIVE	Drive Type			AFE	0		Unit Select	
	6 — HEAD	Head Address							
	7 — SECT	Sector Address							
	8 — CYLL	Cylinder Address Low Byte							
	9 — CYLH	0					Cyl. Addr. High		
	A — SCNTL	Sector Count Low Byte							
	B — SCNTH	Sector Count High Byte							
	C — DATAL	Data Transfer Address Low Byte							
	D — DATAH	Data Transfer Address High Byte							
	E — DATARL	Data Transfer Relocation Address Low Byte							
	F — DATARH	Data Transfer Relocation Address High Byte							
	10 — HDOFST	ESD	Head Offset						
	11 — RES	0							
	12 — NIOPL	Next IOPB Address Low Byte							
	13 — NIOPH	Next IOPB Address High Byte							
	14 — ECCMH	ECC Pattern High	0						
	15 — ECCML	ECC Pattern Low							
	16 — ECCAL	ECC Offset Byte Low							
Byte	17 — ECCAH	ECC Offset Byte High							

Required for Execution Returned Value

x-917

5.6.7.2 Detailed Description of Drive Clear (Command Code 6)

The Drive Clear command issues a fault clear command to the disk drive and then issues a Re-calibrate command. The Re-calibrate command is a form of Seek; therefore, the the iSBC 226 board completes the IOPB only when the disk drive has completed its Seek.

5.6.8 WRITE FORMAT (COMMAND CODE 7)

The Write Format command formats a disk with header information. The iSBC 226 board writes header information on the disk; crossing sector, head, and cylinder boundaries as required. When the Sector Count reaches zero, the IOPB is posted as complete.

To use the Sector Slip function, the drive must be configured properly and software must issue a Set Drive Size command to the iSBC 226 board (see Section 5.6.12).

5.6.8.1 IOPB

FORMAT

Byte		Bit Number → 7	6	5	4	3	2	1	0
0	COMM	AUD	RELO	CHEN	IEN	Command Code			
1	IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
2	STAT1	ERRS	0		Controller Type			0	DONE
3	STAT2	Error or Completion Code							
4	THROT	BWM	Interleave Factor				Throttle		
5	DRIVE	Drive Type			AFE	0		Unit Select	
6	HEAD	Head Address							
7	SECT	Sector Address							
8	CYLL	Cylinder Address Low Byte							
9	CYLH	0					Cyl. Addr. High		
A	SCNTL	Sector Count Low Byte							
B	SCNTH	Sector Count High Byte							
C	DATAL	Data Transfer Address Low Byte							
D	DATAH	Data Transfer Address High Byte							
E	DATARL	Data Transfer Relocation Address Low Byte							
F	DATARH	Data Transfer Relocation Address High Byte							
10	HDOFST	ESD	Head Offset						
11	RES	0							
12	NIOPL	Next IOPB Address Low Byte							
13	NIOPH	Next IOPB Address High Byte							
14	ECCMH	ECC Pattern High	0						
15	ECCML	ECC Pattern Low							
16	ECCAL	ECC Offset Byte Low							
Byte 17	ECCAH	ECC Offset Byte High							

Required for Execution Returned Value

x-918

5.6.8.2 Allocating Spare Sectors

Determine both the maximum number of sectors per track available on the drive and the number of sectors per track you wish to allocate to be spares. Set the disk drive sector switches for the maximum number of sectors per track. The disk drive size set by the Set Drive Size command must equal the total number of sectors per track, minus the number of sectors allocated as spares.

For example, if the disk drive supports 34 sectors per track, set the drive sector switches to 34. If you are allocating 2 sectors per track as spares, set the drive size to 32 sectors per track. This automatically allocates 2 sectors as spares.

5.6.8.3 Implied Seeks

The iSBC 226 board issues an Implied Seek on a Format command. This seek is issued as the first operation after the IOPB is read from system memory. If command-chaining is implemented and the EEF bit is set, the iSBC 226 board scans the remainder of the chain for the possibility of Overlap Seeks.

5.6.8.4 Filling Buffer

When the seek is completed, the iSBC 226 board accesses the IOPB to determine the command parameters and begins to fill the buffer. The iSBC 226 board fills its own internal buffer for use by the format command. The only DMA activity during a Format command is that of reading and updating IOPBs.

5.6.8.5 Test Track Size

When the Seek is completed, the iSBC 226 board accesses the IOPB and determines if the Sector Count and Size is within limits. It does this by timing a track, counting sector pulses, and checking the size of the last sector. The iSBC 226 board performs this once per drive per unit select, as part of the Format function . The iSBC 226 board determines if there are spare or runt sectors on each track, and formats them accordingly.

5.6.8.6 Sector Coincidence

The iSBC 226 board waits for the index pulse, and then counts the appropriate number of sector pulses until the sector to be formatted arrives under the heads.

NOTE

If you are interleaving the disk, software must specify the interleave factor at format time, so that the iSBC 226 board can format the sectors in the proper sequence. Formats should start at Sector Ø, and do full multiples of tracks to ensure format integrity while interleaving.

5.6.8.7 Write Header and ECC

After the iSBC 226 board senses the sector pulse for the requested sector, the disk sequencer counts the appropriate number of bytes and then writes the sync bits. It then takes the header words out of the FIFO, serializes them, generates a new ECC value, and writes the header to the disk. The ECC value generated for the header words becomes part of the header on the disk.

5.6.8.8 Sector Data

The iSBC 226 board writes all zeros to the data field portion of the sector.

5.6.8.9 Incrementing Disk Address

The sector address is incremented by 1. If the sector address is greater than max sector, it is reset to zero and the head address is incremented. If the resultant head address is greater than maximum head, then the head address is reset to zero and the cylinder address is incremented by one. If the cylinder is greater than max cylinder when the implied seek is issued, an error is generated.

5.6.8.10 Complete a Transfer

The sector count decrements by 1 each time the disk passes over a sector boundary during formatting. The iSBC 226 board tests the sector count at the end of each sector to determine if the transfer is complete. If the transfer is not complete, the next sector is formatted. An implied seek is issued if the cylinder address increments.

When the iSBC 226 board completes the transfer, the two status bytes of the IOPB are updated, and if interrupts are enabled, an interrupt is generated. If AUD of the IOPB command byte is set, the iSBC 226 board updates the IOPB.

The iSBC 226 board stops a transfer that ends in a hard error, and marks it as complete with error. Any chained operations are terminated. The IOPB address and relocation registers point to the IOPB which caused the error.

If the transfer ends with a soft error, the iSBC 226 board continues any chained operations.

5.6.9 READ HEADER, DATA AND ECC (COMMAND CODE 8)

The Read Header, Data and ECC command reads sectors from the disk into the memory locations specified by the Data Address. The iSBC 226 board reads an additional eight bytes for each sector (see Table 5-4). Software must specify the interleave factor for the iSBC 226 board to read the sectors in the correct sequence from the drive.

5.6.9.1 IOPB

READ H D E

Byte	Bit Number → 7	6	5	4	3	2	1	0
0 — COMM	AUD	RELO	CHEN	IEN	Command Code			
1 — IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
2 — STAT1	ERRS	0		Controller Type			0	DONE
3 — STAT2	Error or Completion Code							
4 — THROT	BWM	Interleave Factor				Throttle		
5 — DRIVE	Drive Type			AFE	0		Unit Select	
6 — HEAD	Head Address							
7 — SECT	Sector Address							
8 — CYLL	Cylinder Address Low Byte							
9 — CYLH	0					Cyl. Addr. High		
A — SCNTL	Sector Count Low Byte							
B — SCNTH	Sector Count High Byte							
C — DATAL	Data Transfer Address Low Byte							
D — DATAH	Data Transfer Address High Byte							
E — DATARL	Data Transfer Relocation Address Low Byte							
F — DATARH	Data Transfer Relocation Address High Byte							
10 — HDOFST	ESD	Head Offset						
11 — RES	0							
12 — NIOPL	Next IOPB Address Low Byte							
13 — NIOPH	Next IOPB Address High Byte							
14 — ECCMH	ECC Pattern High				0			
15 — ECCML	ECC Pattern Low							
16 — ECCAL	ECC Offset Byte Low							
Byte 17 — ECCAH	ECC Offset Byte High							

Required for Execution Returned Value

x-919

NOTE

The sector address specified in the IOPB is an absolute number, and does not take into consideration any slipped sectors.

5.6.9.2 Implied Seeks

The iSBC 226 board issues an implied seek on a Read Header, Data, ECC command. The seek is issued as the first operation after reading the IOPB from system memory. If chained operations are implemented, and the EEF bit is set, the iSBC 226 board scans the remainder of the chain for the possibility of overlap seeks.

5.6.9.3 Seek End

The iSBC 226 board scans the drives, and determines when each drive has completed its seek.

5.6.9.4 Sector Coincidence

The iSBC 226 board waits for the index pulse from the drive, counts the appropriate number of sector pulses (to locate the specified sector), and then reads the sector. System software must specify the interleave factor in the IOPB.

5.6.9.5 Read Data

The disk sequencer waits for the sync bits of the header field. As the iSBC 226 board reads the header from the disk, it de-serializes the header and places into the FIFO buffer. After the iSBC 226 board reads two header words into the FIFO buffer, the disk sequencer waits for the sync bits of the data field. After synchronizing with the data field, the iSBC 226 board reads the data in, de-serializes it, and puts into the FIFO buffer. The last two words read are the ECC words from the end of the data field. When data becomes available at the other end of the FIFO buffer, the iSBC 226 board requests the bus and transfers the data to memory. The iSBC 226 board transfers an additional eight bytes per sector which are the header and ECC fields.

5.6.9.6 Throttle

The throttle is the maximum number of transfers that can occur each time the iSBC 226 board becomes the bus master. On a read operation, the first DMA requests will be at minimum value, because the limiting factor of the burst length is the number of words available from the FIFO buffer. After the initial few DMA bursts, the typical burst length increases, possibly approaching the throttle limit. Words continue to be transferred from the controller as required until the sector count overflows and the buffer is empty.

5.6.9.7 ECC

This command does not support ECC. The iSBC 226 board reads back the two ECC words written on the sector and places them into memory as data.

5.6.9.8 Incrementing Disk Address and Cylinder

After the iSBC 226 board reads a sector, the sector address increments by one. The head addresses do not increment on this command.

5.6.9.9 Completing a Transfer

At the end of each sector, the iSBC 226 board decrements the sector count and tests it to determine if the transfer is complete. If the transfer is not complete, the next sector is transferred. If the sector address is greater than the physical number of sectors on the disk, a Disk Sequencer error occurs. When the iSBC 226 board completes the transfer, it updates the Status Bytes of the IOPB, and if interrupts are enabled, generates an interrupt. If the AUD bit of the IOPB Command Byte is set, the iSBC 226 board updates the IOPB.

The iSBC 226 board stops a transfer that ends with a hard error, updates the status bytes of the IOPBs, and if interrupts are enabled, an interrupt is generated. If the AUD of the IOPB command byte is set, the the iSBC 226 board updates the IOPB.

If the transfer ends with a soft error, the iSBC 226 board updates the two status bytes of the IOPB are updated, and if interrupts are enabled, an interrupt is generated. Any chained operations continue. If AUD is set, the iSBC 226 board updates the IOPB. The ERR bit in the CSR does not set on a soft error.

Table 5-4. Header, Data, and ECC Bytes

Description	Sector Size and Bytes Within a Sector	
	1Ø24 Bytes	N-Bytes
Cylinder Address Low	1	1
Cylinder Address High and Sector Address 64/128	2	2
Head Number	3	3
Sector and Drive Type	4	4
Sector Data	5-1Ø28	5-N+4
Data ECC	1Ø29-1Ø32	(N+5)-(N+8)

5.6.10 READ DRIVE STATUS (COMMAND CODE 9)

The Read Drive Status command posts iSBC 226 board configuration information, and also posts specific drive type information for the drive selected.

5.6.10.1 IOPB

READ DRIVE STATUS

Byte		Bit Number → 7	6	5	4	3	2	1	0
	0 — COMM	AUD	RELO	CHEN	IEN	Command Code			
	1 — IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
	2 — STAT1	ERRS	0		Controller Type			0	DONE
	3 — STAT2	Error or Completion Code							
	4 — THROT	BWM	Interleave Factor				Throttle		
	5 — DRIVE	Drive Type			AFE	0		Unit Select	
	6 — HEAD	Head Address							
	7 — SECT	Sector Address							
	8 — CYLL	Cylinder Address Low Byte							
	9 — CYLH	0					Cyl. Addr. High		
	A — SCNTL	ONCL	DRDY	WRPT	DPB	SKER	DFLT	RSRVD	RSRVD
	B — SCNTH	Firmware Revision Level							
	C — DATAL	Bytes per Sector Low							
	D — DATAH	Bytes per Sector High							
	E — DATARL	Actual Sectors per Track							
	F — DATARH	Data Transfer Relocation Address High Byte							
	10 — HDOFST	ESD	Head Offset						
	11 — RES	0							
	12 — NIOPL	Next IOPB Address Low Byte							
	13 — NIOPH	Next IOPB Address High Byte							
	14 — ECCMH	ECC Pattern High	0						
	15 — ECCML	ECC Pattern Low							
	16 — ECCAL	ECC Offset Byte Low							
Byte	17 — ECCAH	ECC Offset Byte High							

Required for Execution Returned Value

x-920

5.6.10.2 Detailed Description of Read Drive Status (Command Code 9)

The Read Drive Status command has two purposes: it indicates the current size of the drive type specified, and it also indicates the status of the drive unit specified. The IOPB must contain the drive type and unit number. The returned values are in bytes 6H through EH, and 1ØH, of the resulting IOPB. This command does not require the drive type to match the unit number of a disk drive.

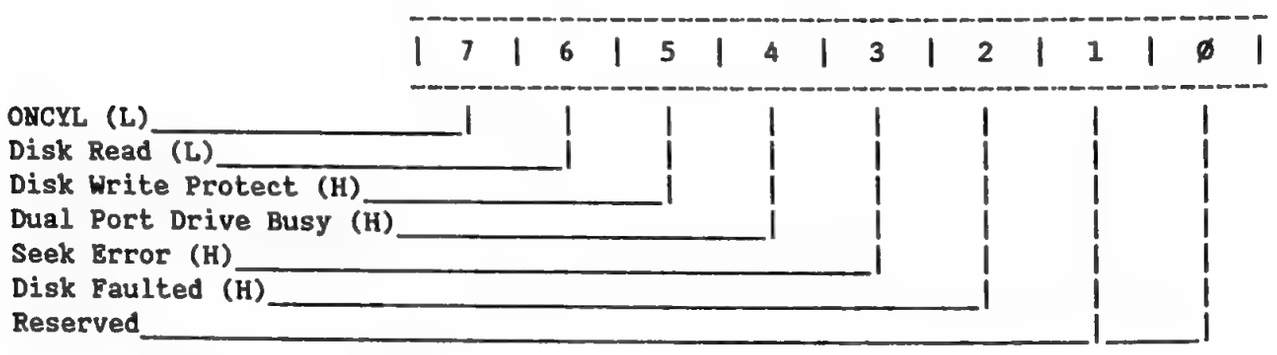
5.6.10.3 Returned Values

Executing a Read Drive Status command returns the following information in the IOPB:

Drive Type Specified	iSBC 226 Board	Selected Drive
Maximum Sector	Code Revision	Drive Status
Maximum Head	Sector Size	Number of Sectors/Track
Maximum Cylinder	Adaptive Format Enable	
Head Offset		
Embedded Servo Drive		

5.6.10.4 Drive Status

The iSBC 226 board selects the drive, latches the following information, and releases the drive. Byte ØAH contains the latched drive information.



Bit	Mnemonic	Meaning
7	ONCL	On Cylinder (L) - represents the On Cylinder status of the drive whose drive number is in the Drive byte of this IOPB. If the drive is ready and this bit is zero, this drive is not seeking. If this bit is a one, then the heads of the selected drive are not positioned over a cylinder.
6	DRDY	Disk Read (L) - is zero if the drive selected is ready.
5	WRPT	Disk Write Protect (H) - if set, the selected disk is write-protected.
4	DPB	Dual Port Busy (H) - sets when the iSBC 226 board selects a busy port in a dual port drive. If bit is clear, the selected drive is not busy or not ready.
3	SKER	Hard Seek Error (H) - is set if the selected drive reports a Hard Seek Error in its logic.

5.6.10.4 Drive Status (continued)

Bit	Mnemonic	Meaning
2	DFLT	Disk Fault (H) – if set, the selected drive reports any type of Fault in its logic.
Ø,1	---	Reserved.

5.6.10.5 Drive Type Parameters

The Drive Type parameters are:

- Maximum Head
- Maximum Sector
- Maximum Cylinder
- Head Offset
- Embedded Servo Drive

The parameters of the drive size are loaded into bytes 6H through 9H, and 1ØH. The maximum head value loads into byte 6H, the maximum sector value loads into byte 7H; and the maximum cylinder value loads into bytes 8H and 9H. The value for head offset loads into byte 1ØH. The status of the embedded servo drive (bit 7) also loads into Byte 1ØH (typically ØH for a drive that does not have fixed and removable media).

5.6.10.6 iSBC® 226 Board Parameters

The Read Drive Status command provides the: firmware revision number, sector size in bytes per sector, and adaptive format enable. Byte ØBH contains the revision code where 1=A, 2=B, etc. Bytes ØCH and ØDH contain the number of bytes per sector.

The iSBC 226 board defines bit 4 of IOPB Byte 5 as the Adaptive Format Enable (AFE) bit. This bit indicates the iSBC 226 board is using Adaptive Format (i.e., the sectors are skewed). Bit 4 is always set.

5.6.10.7 Drive Parameters

The iSBC 226 board counts the total number of sectors per track. This number includes all sectors, even if one of the sectors is too small (runt sector) to be a data sector. This count is returned in byte ØEH.

5.6.11 WRITE HEADER, DATA AND ECC (COMMAND CODE A)

This command writes the header, data, and ECC for one or more sectors. The iSBC 226 board takes the header, data, and ECC from memory, as specified by the Data Transfer Address. It then writes eight additional bytes per sector on the disk (Table 5-4 illustrates the order of the sectors). System software must specify the interleave factor for the iSBC 226 board to write sectors in the correct order on the disk.

5.6.11.1 IOPB

WRITE H D E

Byte	Bit Number →	7	6	5	4	3	2	1	0
	0 — COMM	AUD	RELO	CHEN	IEN	Command Code			
	1 — IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
	2 — STAT1	ERRS	0		Controller Type			0	DONE
	3 — STAT2	Error or Completion Code							
	4 — THROT	BWM	Interleave Factor				Throttle		
	5 — DRIVE	Drive Type			AFE	0		Unit Select	
	6 — HEAD	Head Address							
	7 — SECT	Sector Address							
	8 — CYLL	Cylinder Address Low Byte							
	9 — CYLH	0					Cyl. Addr. High		
	A — SCNTL	Sector Count Low Byte							
	B — SCNTH	Sector Count High Byte							
	C — DATAL	Data Transfer Address Low Byte							
	D — DATAH	Data Transfer Address High Byte							
	E — DATARL	Data Transfer Relocation Address Low Byte							
	F — DATARH	Data Transfer Relocation Address High Byte							
	10 — HDOFST	ESD	Head Offset						
	11 — RES	0							
	12 — NIOPL	Next IOPB Address Low Byte							
	13 — NIOPH	Next IOPB Address High Byte							
	14 — ECCMH	ECC Pattern High	0						
	15 — ECCML	ECC Pattern Low							
	16 — ECCAL	ECC Offset Byte Low							
Byte	17 — ECCAH	ECC Offset Byte High							

Required for Execution Returned Value

x-921

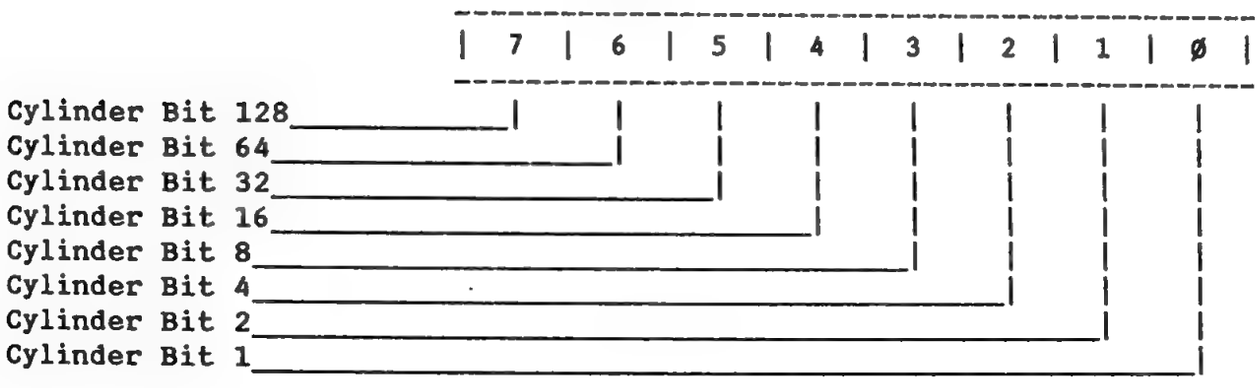
NOTE

The sector address specified in the IOPB is an absolute value and does not take into consideration any slipped sectors.

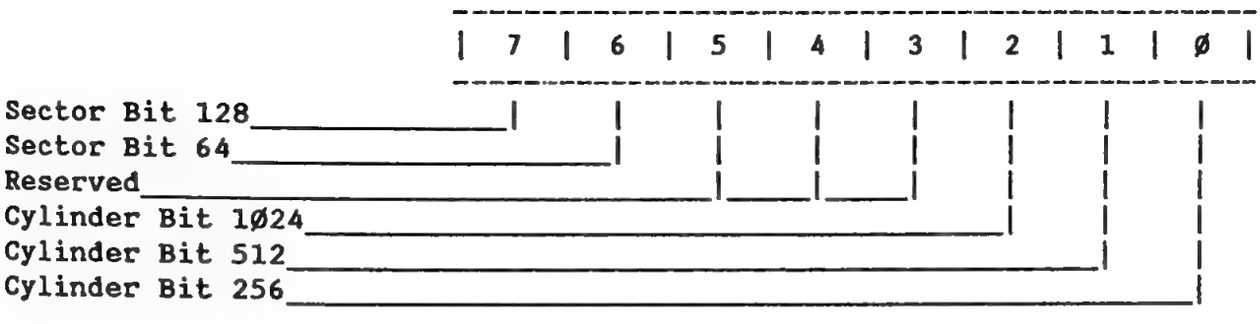
5.6.11.2 Data Buffer

System software must create a data buffer in system memory before issuing the IOPB for a Write Header, Data, and ECC command. The first four bytes in the buffer are the header bytes. The following diagrams show the proper layout for these bytes. The next 1Ø24 bytes (for 1Ø24 byte sectors) are the data to be written on the sector. The last four bytes are the ECC bytes to be written on the sector.

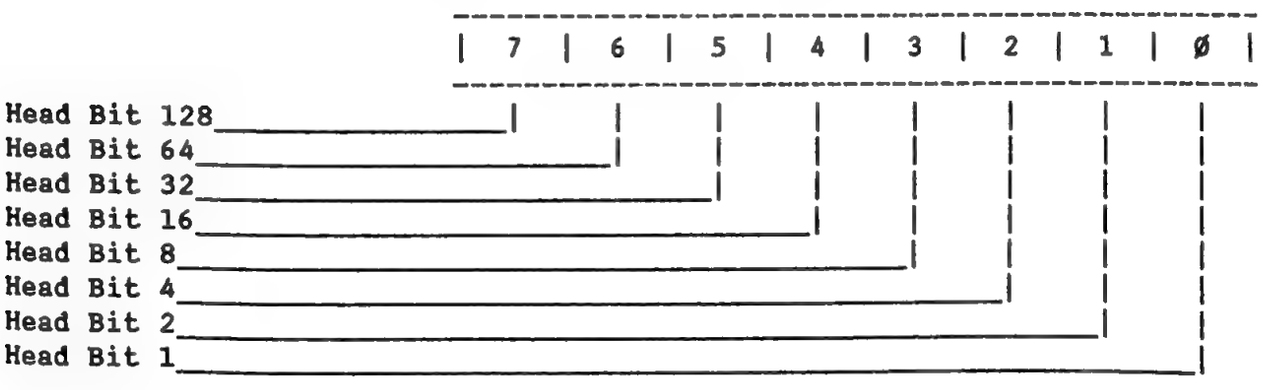
Buffer Byte Ø



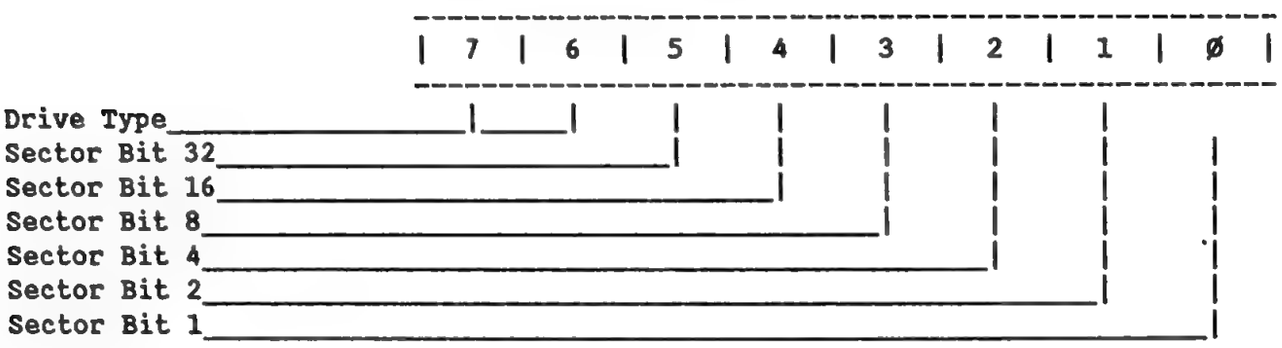
Buffer Byte 1



Buffer Byte 2



Buffer Byte 3



5.6.11.3 Implied Seeks

The iSBC 226 board issues an implied seek on a Write Header, Data and ECC command. The seek is issued as the first operation after reading the IOPB from system memory. If command-chaining is enabled, and the EFF bit is set, the iSBC 226 board scans the remainder of the chain for the possibility of overlap seeks.

5.6.11.4 Filling the Buffer

When the seek is complete, the iSBC 226 board accesses the IOPB to determine the command parameters and begins to fill the buffer. The iSBC 226 board searches for a requested sector when the buffer contains one sector of data. This ensures sufficient data is available in the buffer at the start of the write.

5.6.11.5 Sector Coincidence

The iSBC 226 board waits for an index pulse from the drive, counts the appropriate number of sector pulses (to locate the specified sector), and writes that sector. System software must specify the interleave factor in the IOPB.

5.6.11.6 Write Data

The disk sequencer counts the appropriate number of bytes after sector coincidence and then writes the sync bits. It takes two words out of the FIFO buffer, serializes them, generates a new ECC value; and writes them, and the ECC, to the disk as the new header. The disk sequencer counts an appropriate number of bytes and then writes the data sync bits. It takes the data from the FIFO buffer, serializes it, and writes the data to the disk. As the sequencer removes data from the FIFO buffer, it is replaced by data accessed directly from system memory.

5.6.11.7 Throttle

The throttle is the maximum number of DMA transfers that can occur each time the iSBC 226 board becomes the bus master. On a write operation, the first DMA bursts are at maximum value until the buffer fills. After words start moving to the disk, the typical burst is less than the throttle value. The iSBC 226 board continues transferring data as required, until the sector count overflows.

5.6.11.8 ECC

After the iSBC 226 board writes the data field, it takes the ECC words from the buffer and writes them to the disk.

5.6.11.9 Incrementing Disk Address

The sector address increments by one. This command does not increment the head address.

5.6.11.10 Completing a Transfer

The sector count decrements by one each time the DMA address increments over a sector boundary. The iSBC 226 board test the sector count at the end of a sector to determine if the transfer is complete. If the transfer is not complete, the next sector is transferred. A disk sequencer error occurs if the sector address increments beyond max sector.

When the iSBC 226 board completes the transfer, it updates the two status bytes of the IOPB, and if interrupts are enabled, an interrupt is generated. If AUD of the IOPB command byte is set, the iSBC 226 board updates the IOPB.

The iSBC 226 board stops a transfer that ends with a hard error, and updates the two status bytes of the IOPB. If interrupts are enabled, an interrupt is generated. Any chained operations are halted. The IOPB address and relocation registers point to the IOPB which caused the error. If AUD is set, the iSBC 226 board updates the IOPB.

If the transfer ends with a soft error, the iSBC 226 board updates two status bytes of the IOPB, and if interrupts are enabled, an interrupt is generated. Any chained operations are continued. If AUD is set, the iSBC 226 board updates the IOPB.

5.6.12 SET DRIVE SIZE (COMMAND CODE B)

The Set Drive Size command allows system software to configure the drive size parameters of the iSBC 226 board to operate with drives of any number of sectors, head, and cylinders. System software modifies the parameters for the drive type specified in byte 5H. The new max head value loads into byte 6H, the max sector value loads into byte 7H, the new max cylinder value loads into bytes 8H and 9H, with byte 9H being the most significant. The head offset value and drive servo type, loads into byte 1ØH. If the drive is an Embedded Servo Drive (ESD) type, bit 7 of byte 1ØH must be set.

Bus initialization and power-up reset any size parameters modified by a Set Drive Size command, to the default values in EPROM.

5.6.12.1 IOPB

SET DRIVE SIZE

	Bit Number →	7	6	5	4	3	2	1	0
Byte	0 — COMM	AUD	RELO	CHEN	IEN	Command Code			
	1 — IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
	2 — STAT1	ERRS	0		Controller Type			0	DONE
	3 — STAT2	Error or Completion Code							
	4 — THROT	BWM	Interleave Factor				Throttle		
	5 — DRIVE	Drive Type			AFE	0		Unit Select	
	6 — HEAD	Head Address							
	7 — SECT	Sector Address							
	8 — CYLL	Cylinder Address Low Byte							
	9 — CYLH	0					Cyl. Addr. High		
	A — SCNTL	Sector Count Low Byte							
	B — SCNTH	Sector Count High Byte							
	C — DATAL	Data Transfer Address Low Byte							
	D — DATAH	Data Transfer Address High Byte							
	E — DATARL	Data Transfer Relocation Address Low Byte							
	F — DATARH	Data Transfer Relocation Address High Byte							
	10 — HDOFST	ESD	Head Offset						
	11 — RES	0							
	12 — NIOPL	Next IOPB Address Low Byte							
	13 — NIOPH	Next IOPB Address High Byte							
	14 — ECCMH	ECC Pattern High	0						
	15 — ECCML	ECC Pattern Low							
	16 — ECCAL	ECC Offset Byte Low							
Byte	17 — ECCAH	ECC Offset Byte High							

Required for Execution Returned Value

x-922

5.6.12.2 Disk Sectors Per Track

The IOPB must contain the maximum value of the number of sectors per track, minus one. If the disk you are using has 32 sectors per track, the iSBC 226 board refers to them as sectors Ø-31. Enter 1FH in byte 7 (the hex equivalent of 31).

5.6.12.3 Disk Heads Per Cylinder

The IOPB must contain the maximum value of the number of heads, minus one. If the disk you are using has 19 heads, the iSBC 226 board refers to them as heads Ø-18. Enter 12H in byte 7H.

If you are specifying a drive type for a fixed/removable disk, system software must set the maximum head value for the fixed or removable sections. For example, the drive type that specifies the removable portion of a Control Data Corporation 96 MB SMD disk drive has a maximum head address of ØH, because it has only one head. The drive type that specifies the fixed portion of the disk has a maximum head address of 4H.

5.6.12.4 Disk Cylinders

The IOPB must contain the maximum value of cylinders, minus one. If the disk you are using has 823 cylinders, the iSBC 226 board refers to them as cylinders Ø-822. Enter 36H in byte 8, and 3H in byte 9 (336H is the hex equivalent of 822).

5.6.12.5 Head Offset (IOPB Byte 10H)

The Set Drive Size and Read Drive Status commands use head offset (IOPB Byte 1ØH). This byte determines the offset required to access a fixed or removable section of a disk drive. This byte contains the bits which must be added to the head offset value sent to the drive to select either the fixed or removable portion of the drive.

System software must specify a value for head offset for fixed/removable drives. Software specifies these drives as two different types: one drive type specifies the removable portion of the drive, and the other specifies the fixed portion. The offset value is a hex number that is added to the head number in order to select either the fixed or removable portion of the disk.

For example, the head offset value for the removable portion of a Cartridge Module Drive is ØH, while the head offset value for the fixed portion is 1ØH. In both cases, the drive unit number is Ø for Drive Ø. Refer to the manufacturer's disk drive manual to determine the head offset values for the fixed and removable portions of the disk.

5.6.12.6 Drive Servo Type (IOPB Byte 10H)

When bit 7 of byte 1ØH is set, software selects a seek after every head change, which is required when using an embedded servo disk drive. This seek is required by the drive in order to lock onto the new track. When using an embedded servo drive, the drive should be configured for the mode that requires the controller to issue a seek on each head change. However, it may not be required to set this bit on embedded servo drives that provide this feature automatically. See Section 5.6.1Ø for further detail.

5.6.12.7 Drive Type Usage

The function of defining a drive size parameter is linked to the drive type versus the unit number. The advantage is that only one Set Drive Size command is necessary if all the connecting drives are the same size. Another advantage is that the controller tests for the drive type during a Header Compare operation. The Drive type bits in IOPB byte 5 indicate the size of the drive the iSBC 226 board is working with. There are four drive types available, Ø through 3. The Set Drive Size parameters command allows system software to assign a specific drive type to a specific drive size.

For example, a hypothetical system has two drives. One drive is an 8ØMB disk drive (call it drive type 1), the other is a 3ØØMB disk drive (call this one drive type 2). Execute a Set Drive Size parameters command, using the following parameters to set drive type 1: 5 heads, 823 cylinders, and 32 sectors per track. Drive type 2 uses these parameters: 19 heads, 823 cylinders, and 32 sectors per track. In this hypothetical system, whenever the iSBC 226 board talks to the 8ØMB drive, system software must access it as Drive Type 1 (along with the required unit number). System software refers to the 3ØØMB drive as Drive Type 2 and selects the unit number.

5.6.12.8 Test Drive Types

The drive type is composed of two bits in the sector header field of each sector on the disk (refer to Figure 5-5. Sector Format). The iSBC 226 board compares the drive type bits with the connected drives during a Header Compare operation to check the validity of the transfer. A Header not Found error occurs when the user-specified drive type (in the IOPB), and the drive type in the sector header, do not match.

5.6.12.9 Default Parameters

Bus initialization, power-up, and self test reset the size parameters to the default parameters in EPROM. Table 5-5 provides the default parameters.

Table 5-5. Default Size Parameters

Drive Type (Byte 5)	Heads (Byte 6)	Sector (Byte 7)	Cylinder (Byte 8,9)	Drive (Mfg.) (Model)	Capacity (MB)
Ø	19	32	823	CDC 9766	3ØØ
1	5	32	823	CDC 9762	8Ø
2	2Ø	46	842	Fujitsu 2351	474
3	255	128	2Ø47	(Maximum Config.)	XXX

Note: CDC is an acronym for Control Data Corporation.
Head Offset (Byte 1ØH) is Ø for all drive types (Ø - 3).

5.6.13 SELF TEST (COMMAND CODE C)

The Self Test command starts the same self test that is run automatically on power-up. If successfully completed, a success status is reported. If the board is not functioning properly, the self test LED will not extinguish, and the appropriate error status is reported. Only use this command if command-chaining is disabled.

5.6.13.1 IOPB

SELF TEST

Byte		Bit Number → 7	6	5	4	3	2	1	0
Byte	0 — COMM	AUD	RELO	CHEN	IEN	Command Code			
	1 — IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
	2 — STAT1	ERRS	0		Controller Type			0	DONE
	3 — STAT2	Error or Completion Code							
	4 — THROT	BWM	Interleave Factor				Throttle		
	5 — DRIVE	Drive Type			AFE	0		Unit Select	
	6 — HEAD	Head Address							
	7 — SECT	Sector Address							
	8 — CYLL	Cylinder Address Low Byte							
	9 — CYLH	0					Cyl. Addr. High		
	A — SCNTL	Sector Count Low Byte							
	B — SCNTH	Sector Count High Byte							
	C — DATAL	Data Transfer Address Low Byte							
	D — DATAH	Data Transfer Address High Byte							
	E — DATARL	Data Transfer Relocation Address Low Byte							
	F — DATARH	Data Transfer Relocation Address High Byte							
	10 — HDOFST	ESD	Head Offset						
	11 — RES	0							
	12 — NIOPL	Next IOPB Address Low Byte							
	13 — NIOPH	Next IOPB Address High Byte							
	14 — ECCMH	ECC Pattern High				0			
	15 — ECCML	ECC Pattern Low							
	16 — ECCAL	ECC Offset Byte Low							
Byte	17 — ECCAH	ECC Offset Byte High							

Required for Execution Returned Value

x-923

5.6.14 DMA TEST (COMMAND CODE D)

The DMA Test command is for diagnostic purposes only. It verifies whether the iSBC 226 board can successfully perform direct memory accesses (DMA) to and from system memory. The DMA Test command reads the first 16 bytes of the IOPB into the iSBC 226 board's FIFO buffer, then writes them directly to the IOPB address plus 32. This command does not update Status Bytes 1 or 2, and does not work if the EEF bit and the Done bits are set at the same time. Clear (zero) IMODE (Byte 1) and STAT1 (Byte 2), before issuing a DMA Test command. Bytes 3 through 17H can be any pattern desired. This command allows fast verification of iSBC 226 board operation before system software is ready to test.

5.6.14.1 IOPB

D M A TEST

Byte		Bit Number → 7	6	5	4	3	2	1	0
	0 — COMM	AUD	RELO	CHEN	IEN	Command Code			
	1 — IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
	2 — STAT1	ERRS	0		Controller Type			0	DONE
	3 — STAT2	Error or Completion Code							
	4 — THROT	BWM	Interleave Factor				Throttle		
	5 — DRIVE	Drive Type			AFE	0		Unit Select	
	6 — HEAD	Head Address							
	7 — SECT	Sector Address							
	8 — CYLL	Cylinder Address Low Byte							
	9 — CYLH	0					Cyl. Addr. High		
	A — SCNTL	Sector Count Low Byte							
	B — SCNTH	Sector Count High Byte							
	C — DATAL	Data Transfer Address Low Byte							
	D — DATAH	Data Transfer Address High Byte							
	E — DATARL	Data Transfer Relocation Address Low Byte							
	F — DATARH	Data Transfer Relocation Address High Byte							
	10 — HDOFST	ESD	Head Offset						
	11 — RES	0							
	12 — NIOPL	Next IOPB Address Low Byte							
	13 — NIOPH	Next IOPB Address High Byte							
	14 — ECCMH	ECC Pattern High	0						
	15 — ECCML	ECC Pattern Low							
	16 — ECCAL	ECC Offset Byte Low							
Byte	17 — ECCAH	ECC Offset Byte High							

Required for Execution Returned Value

x-924

5.6.15 MAINTENANCE BUFFER LOAD (COMMAND CODE E)

The Maintenance Buffer Load command is for diagnostic purposes only. It sets an address in the iSBC 226 board which is used by the Maintenance Buffer Dump command. It is important, to only chain a Maintenance Buffer Load command to a Maintenance Buffer Dump command. To implement a Maintenance Buffer Load command (the buffer is 3ØØH bytes long), write a pattern in memory, starting at the specified Buffer address.

This command will not function properly in chained mode, unless chained only to one Buffer Dump IOPB.

5.6.15.1 IOPB

BUFFER LOAD

Byte		Bit Number → 7	6	5	4	3	2	1	0
	0 — COMM	AUD	RELO	CHEN	IEN	Command Code			
	1 — IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
	2 — STAT1	ERRS	0		Controller Type			0	DONE
	3 — STAT2	Error or Completion Code							
	4 — THROT	BWM	Interleave Factor				Throttle		
	5 — DRIVE	Drive Type			AFE	0		Unit Select	
	6 — HEAD	Head Address							
	7 — SECT	Sector Address							
	8 — CYLL	Cylinder Address Low Byte							
	9 — CYLH	0					Cyl. Addr. High		
	A — SCNTL	Sector Count Low Byte							
	B — SCNTH	Sector Count High Byte							
	C — DATAL	Data Transfer Address Low Byte							
	D — DATAH	Data Transfer Address High Byte							
	E — DATARL	Data Transfer Relocation Address Low Byte							
	F — DATARH	Data Transfer Relocation Address High Byte							
	10 — HDOFST	ESD	Head Offset						
	11 — RES	0							
	12 — NIOPL	Next IOPB Address Low Byte							
	13 — NIOPH	Next IOPB Address High Byte							
	14 — ECCMH	ECC Pattern High				0			
	15 — ECCML	ECC Pattern Low							
	16 — ECCAL	ECC Offset Byte Low							
Byte	17 — ECCAH	ECC Offset Byte High							

Required for Execution Returned Value

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5.6.16 MAINTENANCE BUFFER DUMP (COMMAND CODE F)

The Maintenance Buffer Dump command is for diagnostic purposes only. The iSBC 226 board transfers directly from memory exactly 3ØØH bytes of data (from the address specified in the Maintenance Buffer Load command) into the FIFO buffer. After the DMA is complete, the iSBC 226 board transfers the data from the buffer directly back to the memory address specified in this command. Remember, only chain a Maintenance Buffer Dump command to a Maintenance Buffer Load command (before chaining, reset the EEF bit).

5.6.16.1 IOPB

BUFFER DUMP

Byte	Bit Number →	7	6	5	4	3	2	1	0
	0 — COMM	AUD	RELO	CHEN	IEN	Command Code			
	1 — IMODE	0	IEI	IERR	HDP	ASR	EEF	ECC Mode	
	2 — STAT1	ERRS	0		Controller Type			0	DONE
	3 — STAT2	Error or Completion Code							
	4 — THROT	BWM	Interleave Factor				Throttle		
	5 — DRIVE	Drive Type			AFE	0		Unit Select	
	6 — HEAD	Head Address							
	7 — SECT	Sector Address							
	8 — CYLL	Cylinder Address Low Byte							
	9 — CYLH	0						Cyl. Addr. High	
	A — SCNTL	Sector Count Low Byte							
	B — SCNTH	Sector Count High Byte							
	C — DATAL	Data Transfer Address Low Byte							
	D — DATAH	Data Transfer Address High Byte							
	E — DATARL	Data Transfer Relocation Address Low Byte							
	F — DATARH	Data Transfer Relocation Address High Byte							
	10 — HDOFST	ESD	Head Offset						
	11 — RES	0							
	12 — NIOPL	Next IOPB Address Low Byte							
	13 — NIOPH	Next IOPB Address High Byte							
	14 — ECCMH	ECC Pattern High				0			
	15 — ECCML	ECC Pattern Low							
	16 — ECCAL	ECC Offset Byte Low							
Byte	17 — ECCAH	ECC Offset Byte High							

Required for Execution Returned Value

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5.7 HOW TO PROGRAM THE iSBC® 226 BOARD

This section of the manual deals with several methods of programming the iSBC 226 (SMD) Disk Controller board. In the following sections, it is assumed that interrupts are enabled. Ignore the references to interrupts if they are not enabled in your situation.

5.7.1 IOPB PROCESSING WITH NO COMMAND CHAINING

Use the following steps when processing an IOPB with no command chaining:

- **Set up IOPB** — Allocate a 24 byte long segment of memory to build an IOPB. Set the various bytes in this IOPB as required to perform a function. Refer to Section 5.5.
- **Point iSBC 226** — Write the address of the IOPB into the iSBC board to IOPB 226 board IOPB address registers.
- **Set Go** — Write 8ØH (GBSY - this is the Go/Busy Bit) to the Control Status Register (CSR). This starts the operation. The host processor either polls the CSR for DONE, or waits for the interrupt.
- **The iSBC 226 Board Processing** — The iSBC 226 board starts to process the IOPB after it detects that the GBSY bit has been written into its Control and Status Register. It uses the Address and Relocation Registers to address MULTIBUS memory and read the IOPB. It executes the function, and when complete, will update the status bytes of the IOPB, reset the GBSY bit, and interrupt.

NOTE

It is not recommended to wait for DONE in STAT1 because it sets while the controller is busy.

The iSBC 226 board starts processing the IOPB after it detects the GBSY bit has been written to the CSR. It uses the Address and Relocation Registers to address MULTIBUS memory and read the IOPB. It executes the function called for; and when complete, updates the Status Bytes of the IOPB, resets the GBSY bit, and interrupts.

- **Check for Errors** — Read both the CSR, and Status Byte 2 to determine if the command completed without error. Test the CSR to determine if the DERR is set, as this may indicate the status byte 2 was not updated. If DERR is not set, check ERR and the value in status type 2; if they are zero, the command completed successfully. Any other value indicates an error situation.

  The completion code of a command appears in status byte 2. A code of Ø indicates successful completion, any other value indicates an error status. Error codes are listed in Section 5.4.4. Section 5.7.3 explains error recovery.

5.7.2 IOPB PROCESSING WITH COMMAND CHAINING ENABLED

The iSBC 226 board supports IOPB chaining so that multiple IOPBs may be queued and executed as fast as possible. The chain starts with the IOPB Address Registers pointing to the IOPB, and follows the address pointers in each IOPB to the next IOPB. The iSBC 226 board completes all IOPBs, or stops the chain when a hard error is detected. If the EEF bit is set, the iSBC 226 board scans the IOPB chain and issues seek commands to units not busy (the commands may not be executed in the order in which they were chained).

5.7.2.1 The Chain

Each IOPB has a field which points to the next IOPB in the chain. The iSBC 226 board does not look at the chain pointer unless CHEN in the command byte is set. The IOPB relocation registers relocate the next IOPB address bytes. Therefore, all IOPBs in a chain must be located within the 64 KB memory block starting at the base address in the IOPB relocation register.

5.7.2.2 Executing the Chain with Overlapped Seeks

Each time the iSBC 226 board starts, or after each Attention Request (with Overlap Seeks enabled), the controller scans the IOPB list for incomplete IOPB requests for disks which are not busy. It analyzes the first unprocessed request for a non-busy disk, and if it is a seek, read, or write command, the iSBC 226 board initiates a seek (which moves the heads to the correct cylinder). This occurs for both disk drives.

When each drive reaches the desired cylinder, the iSBC 226 board initiates the requested data transfer for that drive. Seek commands are complete at this point. If the EEF bit is set, IOPBs complete in the order in which their seeks are completed.

If you are chaining commands, and the EEF and DONE bits are set, software must clear STAT 1 and STAT 2 before re-issuing the IOPB.

5.7.2.3 Completing IOPBs

As each IOPB is completed, the status bytes in the IOPB update along with the completion code. If the Interrupt on Each bit (IEI) is set, the iSBC 226 board interrupts as it completes each IOPB. The iSBC 226 board acknowledges an interrupt by writing a one into the Interrupt Pending Bit (IPND) of the CSR. Do not reset the Interrupt Pending and/or Error bits with a Controller Reset, as this may cause drive faults and misposition errors when the iSBC 226 board continues the chain. The iSBC 226 board remains busy until either the chain is complete, or a hard error occurs.

5.7.2.4 Modifying the Chain During Execution

The iSBC 226 board's Attention protocol uses tow bits in the Controller Status Register: Attention Request (AREQ) and Attention Request Acknowledge (AACK). System software must set the Attention Request bit (AREQ) to notify the iSBC 226 board that it wishes to add or remove IOPBs from the chain. When the iSBC 226 board recognizes this request it sets the Attention Request Acknowledge bit (AACK) in the Controller Status Register. If the IEI bit is set, an interrupt occurs.

System software may now remove IOPBs that have been marked as complete, and/or may add new IOPBs to the queue. IOPBs that were queued previously but are not marked complete (you may modify CHEN and the next IOPB address, but do not touch previously queued IOPBs that are not marked complete).

5.7.2.5 Restarting a Modified Chain

When system software has completed adding or removing IOPBs, it clears AREQ and the iSBC 226 board clears (AACK). At this point, make sure the GBSY bit is still set. Due to processing delays, GBSY may be set when software clears AREQ (if the iSBC 226 board determines the IOPB chain is complete when is sets AACK, it may clear GBSY). If GBSY is set, the iSBC 226 board continues processing the IOPB chain. If GBSY is clear, set it to start a new chain.

5.7.2.6 Chain Interrupts

The iSBC 226 board provides a single interrupt at the end of each IOPB. Thus, interrupts occur after the iSBC 226 board has: completed a single IOPB, completed several chained IOPBs, or granted AACK. System software must determine why the interrupt occurred, and if it occurred for multiple interrupt requests. If three IOPBs complete at the same time, the iSBC 226 board generates only a single interrupt. The iSBC 226 board assumes that any complete IOPB has been taken care of by system software (at the time of setting GBSY or IPND, or the time of resetting of AREQ).

5.7.2.7 Completing the Chain

When all IOPBs in a chain are complete, the chain is complete. If one IOPB has a hard error, the chain terminates with an error. If interrupts are enabled, an interrupt occurs. If the chain completes successfully with the EEF and IEI bits set, the iSBC 226 board remains busy until it re-scans the entire chain, ensuring all IOPBs are complete before it clears the GBSY bit.

5.7.3 ERROR RECOVERY

Various procedures may recover certain errors. The following errors are grouped according to the recommended software recovery procedure.

5.7.3.1 Errors 01H, 03H, 07H, 0AH, 17H, 19H, 1AH, and 20H

These errors are either programming errors or hard failures. Do not retry the operation.

Code	Description
Ø1H	Interrupt Pending
Ø3H	Busy Conflict
Ø7H	Illegal Cylinder Address
ØAH	Illegal Sector Address
17H	Sector Count Zero
19H	Illegal Sector Size
1AH	Self Test
2ØH	Illegal Head Address

5.7.3.2 Errors 04H, 05H, 06H, 16H

Retrying the operation may recover these errors. Execute two retries. If the error persists, consider it unrecoverable.

Code	Description
Ø4H	Operation Time Out
Ø5H	Header Not Found
Ø6H	Hard ECC Error
16H	Drive Not Ready

5.7.3.3 Errors 12H, 18H, and 25H

These errors indicate the drive may be off cylinder. Issue a Drive Clear and then retry the transfer. This can be accomplished automatically by setting the ASR bit in byte 1.

Code	Description
12H	Cylinder and Head Header Error
18H	Drive Faulted
25H	Hard Seek Error

5.7.3.4 Error 0EH

The iSBC 226 board attempted to access non-existent memory. Check the parameters issued, correct them, and try again.

Code	Description
ØEH	Slave ACK Error

5.7.3.5 Errors 0DH and 19H

These errors occur during the format and indicate that the drive may be configured for an improper number of sectors. Verify the sector switches on the drive and the drive size for this drive type.

Code	Description
ØDH	Last Sector Too Small
19H	Illegal Sector Size

5.7.3.6 Errors 13H, 14H and 1FH

Software may log these errors for information purposes only.

Code	Description
13H	Seek Retry Required
14H	Write Protect Error
1FH	Soft ECC Recovered Error

5.7.3.7 Error 1EH

This error occurs when the iSBC 226 board encounters an ECC recoverable error.

Code	Description
1EH	Soft ECC Error

System software may recover the operation as follows:

For a byte-oriented system (ex: 8Ø8Ø or 8Ø85), use the following procedure:

1. Reserve 24 bits of storage for the ECC mask (3 bytes) and initialize them to zero.

2. Take the mask word from the IOPB, reverse its bit, and save the result in the least significant 16 bits of the storage allocated in step 1.

3. Get the bit address word from the IOPB and subtract one (1). Since the bit address always starts at 1, this causes the start to be at bit Ø.

4. Shift the stored mask left using the least significant three bits of the adjusted bit address from step 3 as a count. These three bits are the starting bit number within the byte.

5. Divide the bit address by eight (by performing three logical shifts to the right). The result is the byte offset into the data field where the stored mask is Exclusive Or'ed with the data. Add this to the address of the start of the BAD sector to create a pointer to the first data byte to be corrected.

6. EXclusive OR the data bytes in ascending order, with the three mask bytes using the least significant mask byte to be first.

For word-oriented systems the procedure differs:

1. Reserve 32-bits of storage for the ECC mask (two words) and initialize to zero.

2. Reverse the bit order of the ECC mask word, and save the result in the least significant word of the two-word mask storage allocated in step 1.

3. Get the ECC bit address from the IOPB and subtract 1 to cause the bit count to start at Ø rather than 1.

4. Shift the stored address mask bits left, using the four low order bits of the adjusted ECC address of Step 3 as a count.

5.7.3.7 Error 1EH (continued)

5. Divide the bit address by 16 (by performing four logical shifts to the right). The result is the word offset into the BAD sector. Adding this offset to the start of a sector memory address creates a pointer to the first word to be corrected.

6. EXclusive OR two consecutive words in the data with the mask.

5.7.4 FORMATTING DISK DRIVES

This section is a brief description of the steps to perform when formatting a disk.

5.7.4.1 Set Drive Size Parameters

In order to format the disk, the iSBC 226 board must know the drive size parameters, number of sectors per track, number of heads per cylinder, and number of cylinders. Perform the Set Drive Size Command (Section 5.6.12). This allows the drive size parameters to be set on a per drive basis. Set the number of sectors per track in the drive size parameters equal to the number of sectors in an entire track (or use the default drive size parameters). Do not subtract the number of sectors to be used as spares (for later sector slips).

5.7.4.2 Format the Disk

Format the disk using the Write Format command. Record the sector status by building a table in system memory with two variables, one variable being the physical sector number from the index pulse, and the other variable being the status of that sector (good or bad). Allocate a buffer in system memory, and fill this buffer with the desired data pattern. Write, Read, and Verify the data. As system software verifies the disk, it must record (in the table) all media defects encountered. You may want to use several different patterns to ensure system software finds all the media defects. Recommended patterns include (hexadecimal values):

ØAAAAH
ØFFFFH
ØEBD6H
ØAF5BH
5EB7H
6DB6H

5.7.5 SECTOR SLIP

This section covers the procedure used to slip sectors.

5.7.5.1 Media Defects

Disk drives can produce a soft error in about 1 out of every 10^{10} transfers. A sector is not bad if it fails once with a soft error. Rewrite the pattern and read the sector up to ten times, or until a second error occurs. If only one error occurs, it is not defective and there is no need to slip it. If a second error occurs, add the sector to the bad sector table, and indicate if the error was a bad header, hard ECC, or soft ECC.

5.7.5.2 Reset Drive Size Parameters

Using the Set Drive Size Command (Section 5.6.12), set the drive size parameters equal to the number of data sectors per track desired. This number equals the number of physical sectors the drive can hold, minus the number of spare (slip) sectors desired and the runt sector (if it exists).

5.7.5.3 Reformat the Disk

Use the Write Format Command (Section 5.6.8) to reformat the entire disk, recording in the table, which sectors are spares, and which sectors are bad (refer to Section 5.7.4.2). The iSBC 226 board formats all spare sectors with a header of ØDDDDH, ØDDDDH. If the runt sector exists, it is formatted with a header of ØEEEEH, ØEEEEH.

5.7.5.4 Read Track Headers

System software must allocate a buffer in system memory to store the sector header information during this procedure. The buffer length (in bytes) must be four times the total number of sectors. Issue a Read Track Headers command for the track that contains the sector(s) to be slipped. Table 5-6 shows the data buffer contents after a Read Track Headers Command, and after headers have been modified to show bad sectors.

Table 5-6. Read Track Header Data Buffer Contents

Data	Physical Sector	Logical Sector	Status
36H,Ø3H,Ø4H,4ØH	1	Ø	good
36H,Ø3H,Ø4H,41H	2	1	good
36H,Ø3H,Ø4H,42H	3	2	good
36H,Ø3H,Ø4H,43H	4	3	good
ØEEH,ØEEH,ØEEH,ØEEH	5	–	bad
6H,Ø3H,Ø4H,44H	6	4	good
: , : , : , :	:	:	good
: , : , : , :	:	:	good
36H,Ø3H,Ø4H,5FH	33	31	good
ØDDH,ØDDH,ØDDH,ØDDH	34	–	spare

Note: A data buffer table constructed for the above example would consist of sectors 1-4 good, sector 5 bad (header bytes modified), sectors 6-33 good, and sector 34 as a spare.

5.7.5.5 Spare Sector Available

Determine if enough spare sectors are available. There must be a spare sector available for every sector that software slips.

5.7.5.6 Determine Sector to be Slipped

Determine which sector is to be slipped. First, determine the absolute sector number in relation to the index pulse. Then add the absolute sector number to the number of bad sectors that exist between the index pulse and the sector to be slipped. The absolute sector number equals the logical sector number, if the interleave factor is 1:1 and there are no defective sectors. System software must add in the head number to compensate for the adaptive format.

The interleaving factor must adjust the absolute sector number if the sectors are not contiguous. The following BASIC program determines the interleaving. It provides a vector of interleaved sector numbers such that A(physical)=interleaved.

```
 1Ø      REM INTERLEAVING PROGRAM FOR iSBC 226 BOARD CONTROLLER
 2Ø      DIM A(2ØØ)
 3Ø      REM N = TOTAL NUMBER OF SECTORS PER TRACK
 4Ø      N = 32
 5Ø      REM I = INTERLEAVING FACTOR I:1
 6Ø      I = 2
 7Ø      I9 = ((N-1)/I)+1 \ REM I9 = INTERVAL
 8Ø      I9 = INT(I9)
 9Ø      R = N - ((I9-1)*I)     REM R = REMAINDER
1ØØ      P = Ø \ REM P = PHYSICAL SECTOR
11Ø      I8 = I9 \ REM I8 = INTERVAL COUNT
12Ø      R8 = R \ REM R8 = REMAINDER COUNT
13Ø      B = Ø \ REM STARTING VALUE OF LAST SECTOR
14Ø      L = Ø \ REM LAST SECTOR NUMBER
15Ø      A(Ø) = Ø \ REM FIRST SECTOR MAPPED TO Ø
16Ø      P = P + 1
17Ø      IF P >  (N-1) THEN 29Ø   REM END OF TRACK EXIT
18Ø      L = L + I8
19Ø      R8 = R8 - 1
2ØØ      IF R8 <> Ø THEN 22Ø
21Ø      I8 = I8 -1
22Ø      IF L <= (N-1) THEN 28Ø
23Ø      B = B + 1
24Ø      L = B
25Ø      R8 = R
26Ø      I8 = I9
27Ø      A(P) = L
28Ø      GOTO 16Ø
29Ø      STOP
```

For example, upon reading a track interleaved 2:1 (with Head Zero), system software arranges the sectors as follows:

```
Ø, 16, 1, 17, EEEE, 2, 18, 3, 19, 4, 2Ø, 5, 21, 6, 22, 7, 23, 8, 24,
9, 25, 1Ø, 26, 11, 27, 12, 28, 13, 29, 14, 3Ø, 15, 31, DDDD
```

The sector table described in Section 5.7.5.2 lists sectors 1-4 good, sector 5 bad, sector 6-33 good, and 34 as a spare sector. Software determines logical sector 4 is defective. The algorithm determines the absolute sector number is 9. There is one defective sector between the index pulse and the sector to be slipped; therefore, the physical sector to be slipped is sector 1Ø. The table, with its new entry, reads: sector 1-4 good, sector 5 bad, sectors 6-9 good, sector 1Ø bad, sectors 11-33 good, and 34 as a spare sector.

5.7.5.7 Slip Sectors

Using the table updated in Section 5.7.5.2, and using the vector generated in Section 5.7.5.4, modify the Read Track Header buffer in preparation for the Write Track Headers command. Start at the beginning of the buffer and set up the header for the first sector. The following procedure outlines the steps used to modify the buffer.

1. Get physical sector number to be modified.

2. Multiply this number by four bytes, and add it to the buffer start address to determine where that sector's header begins.

3. Using the table updated in Section 5.7.5.2, modify the four header bytes of all bad sectors with ØEEH, ØEEH, ØEEH, ØEEH. Table 5-6. shows the data buffer contents after the headers have been modified to indicate bad sectors.

NOTE

Spare sectors in Table 5-6 are indicated by the four header bytes being ØDDH, ØDDH, ØDDH, ØDDH (set when the disk was reformatted).

4. If a sector is usable, the first byte is the LSB cylinder, the next byte is the MSB cylinder, the next byte is the head, and the last byte is the new sector number which software ORs with the Drive Type and places into the buffer. See Section 5.6.11.3.

5. Determine the new sector number (using the interleave algorithm), the physical sector number, and the number of bad sectors encountered so far. Subtract the number of bad sectors found between the physical sector number and the index pulse. Use this number to determine the new sector number which software ORs with the Drive Type and placed into the buffer.

6. Continue setting up the buffer for each physical sector on that track. Use the procedure outlined above to determine how to set up each sector.

NOTE

The physical locations of bad sectors must not be moved with relation to the index pulse. The media defects do not move when slipping sectors; therefore, any physical sector marked bad must remain bad. Runt sectors also cannot move in relation to the index pulse.

5.7.5.8 Marking Entire Tracks Defective

If system software marks an entire track defective, it must use a pattern of 7FH in the four header bytes (see Section 5.7.5.7). The iSBC 226 board does not support track slipping.

5.7.5.9 Write Track Headers

Using the Write Tracks Headers Command, system software writes the modified headers to the disk to reformat the track with slipped sectors. Once reformatted, the defective sectors are invisible to the operating system through normal Read and Write commands. The iSBC 226 board can access both good and defective sectors when using Read or Write Headers, Data and ECC.

5.7.5.10 Sector Slip With Live Data

If the disk has live data, the following procedure allows you to slip a sector and not lose the data on the disk. As this procedure requires a full track buffer, it is recommended you use a stand-alone program.

1. Allocate a full track buffer in memory and read a track into memory. Use ECC mode 2 (it corrects the bad data, if possible).

   -OR-

   If a full track buffer is not available in memory, allocate disk space, and store the data in that space.

2. Using the Sector Slip procedure, slip the sector with the error in it.

3. Now, use a normal write command to write the data from the buffer back to the disk. The iSBC 226 board will compensate for slipped sectors.

5.7.6 DUAL PORT DRIVE OPERATION

Dual ported drives require the system software to be more careful in its use of disk space. It is also possible that one of the controllers will not release the drive, preventing the other controller from gaining access. When accessing during file operations, keep the Hold Dual Port bit set, this will hold the drive until the directory updates.

Many disk drives which have a dual port option, also have a protection timeout that releases a channel after a specified time period if the drive is de-selected, but not released. If so desired, you can disable this timeout in the drive (refer to the disk drive manual).

5.7.6.1 Drive Space Allocation

Two different controllers can write to dual ported drives. When system software allocates space on the disk, it is unaware that the another controller may be allocating the same sectors. This can cause two files to trash each other. When using dual ported drives, it is recommended to allow only one controller write access to the disk. If this is impractical, then configure one controller to allocate the space on the disk, and the other to only write into that allocated space.

5.7.6.2 Failure to Gain Access

Occasionally a controller fails to gain access to a dual ported drive. In this case, the operation times out after waiting two seconds after the other IOPBs are complete. The error causes the chain to terminate, and system software may remove any IOPBs for that drive. If a controller attempts to access a dual ported drive while it is busy with another controller, a drive not ready error occurs. Issue a Read Drive Status command to determine the dual port busy status.

5.8 PERFORMANCE CONSIDERATIONS

This section discusses how to optimize performance of the iSBC 226 board. It covers the tradeoffs (their advantages and disadvantages) between various types of operations and configurations.

5.8.1 THROTTLE CONSIDERATIONS

From the iSBC 226 board disk controller's viewpoint, the throttle value should be as high as possible, so that the controller never has to skip revolutions or receive late data errors. However, you may have a real time application that access the bus periodically.

In these applications:

- Determine the maximum time that the iSBC 226 board can be bus master (less time than another unit can be without the bus);
- Determine the response time of your memory, add 5ØØ nano-seconds, and divide that figure into the allowable iSBC 226 board bus master time. The result is the maximum throttle value.
- Pick the figure closest to the iSBC 226 board throttle value without going over the actual amount.

5.8.1.1 High Throttle Advantages

- Maximum disk throughput with minimum missed revolutions.
- Maximum bus throughput with minimum bus overhead.

5.8.1.2 High Throttle Disadvantages

- Tendency to dominate the bus - time critical devices fail.
- Other DMA units may not get enough bus time.

5.8.2 WORD OR BYTE MODE

Word mode transfers are more efficient than byte mode transfers. This is because it takes the same length of time to transfer a word in word mode, as it does a byte in byte mode. Using word mode effectively doubles the iSBC 226 board's throughput.

5.8.2.1 Word Mode Advantages

- Increased throughput with less bus utilization.
- Helps DMA transfers keep up with disk.

5.8.2.2 Word Mode Disadvantages

- Works only on word-oriented memory.

5.8.3 TRANSFERS ON ADDRESS BOUNDARIES

The iSBC 226 board reacts differently to transfers on various address boundaries. Word mode transfers on odd addresses must compensate for the odd address. The iSBC 226 board's internal architecture dictates how transfers across page boundaries are handled.

5.8.3.1 Odd Address Transfer

If you specify an odd address, the iSBC 226 board transfers the data in byte mode, even if word mode was selected.

5.8.3.2 Transfers to Page Addresses

Each time the iSBC 226 board crosses a 256K byte address boundary, the on-board microprocessor updates the upper address bits and restarts the DMA sequencer. Align transfers on address boundaries to minimize this occurrence (this is advantageous if you require the iSBC 226 board's absolute maximum).

5.8.4 INTERLEAVING

Interleaving increases throughput on either a fully loaded system, or one where the operating system response time is slow. Interleaving effectively cuts the disk speed in half for 2:1 interleaving, or a third for 3:1 interleaving, etc.

NOTE

When doing interleaved formatting, it is recommended that you start at a sector address, set the GBSY bit, and format full tracks or multiples of full tracks.

5.8.4.1 Advantages of Interleaving

- Maximum throughput on fully loaded systems.

  Fully loaded systems usually have several DMA devices contending for bus time. In this environment, the iSBC 226 board may fall behind the disk, stop the transfer, and wait one revolution until the next sector arrives under the head. This slows the disk subsystem. If the disk is interleaved, the data rate is much slower. Therefore, the iSBC 226 board's bus requirements are much lower.

- Maximum throughput on slow software systems.

  Slow software systems cannot turn around interrupts in a reasonable amount of time, and usually transfer one sector at a time. In this environment, interleaving can allow the system to catch multiple sectors per revolution, instead of just one as on a non-interleaved disk.

- Less chance of missing revolutions.

5.8.4.2 Disadvantages of Interleaving

- Slows data throughput from the disk by the interleave factor.

5.8.5 CHAINING OPERATIONS

Command-chaining operations results in several performance advantages.

- The iSBC 226 board automatically performs overlap seeking, which has a dramatic performance throughput increase for multi-drive systems.
- The operating system does not have to respond as rapidly at the end of a command; the iSBC 226 board continues to the next command without any operating system intervention.
- The iSBC 226 board allows interrupts at the end of each IOPB, and notifies the system that the IOPB is complete.

5.9 iSBC® 226 BOARD SECTOR FORMAT

See Figure 5-5 for the format and layout of the header bytes.

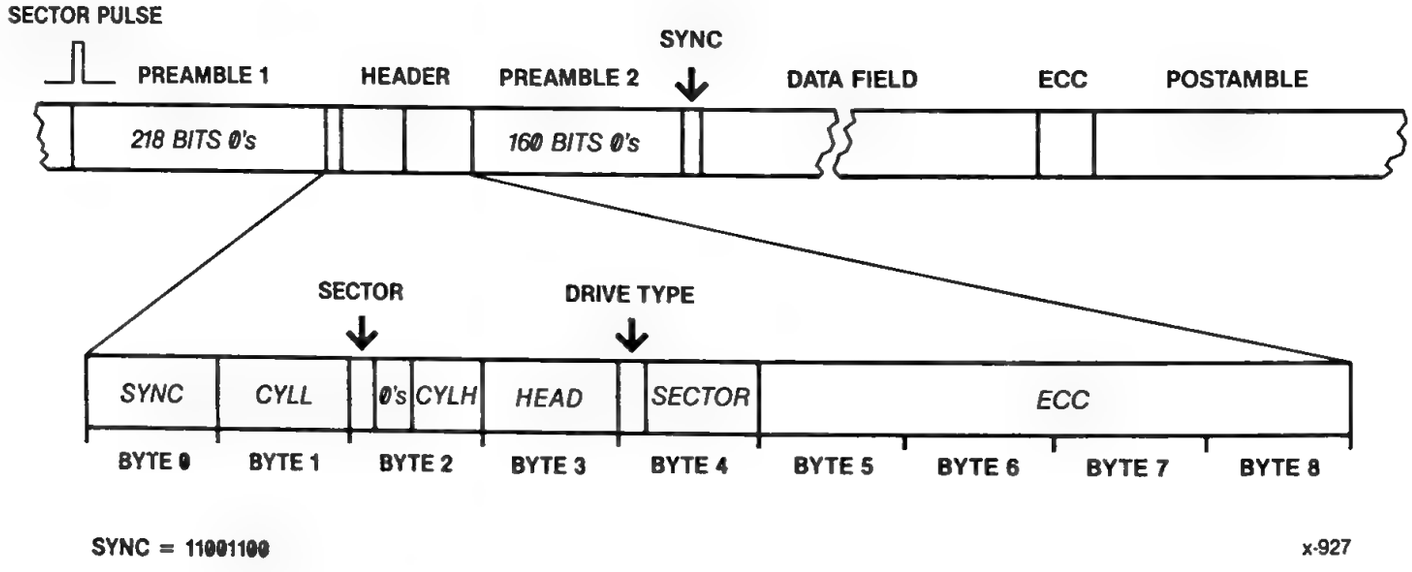

Figure 5-5. iSBC® 226 Board Sector Format

5.10 ADAPTIVE FORMAT

The iSBC 226 board format mode uses adaptive format. The adaptive format causes logical sector zero to slip one sector from the physical index pulse for each track. The logical to physical relationship is reset to 1:1 on track Ø of each cylinder. This feature allows the iSBC 226 board to store more data per track because the adaptive slip masks the head switching time. See Figure 5-6 for the relationship between the index pulse and the logical sector mapping. Figure 5-6 is of a 32-sectored disk with 2 spare sectors.

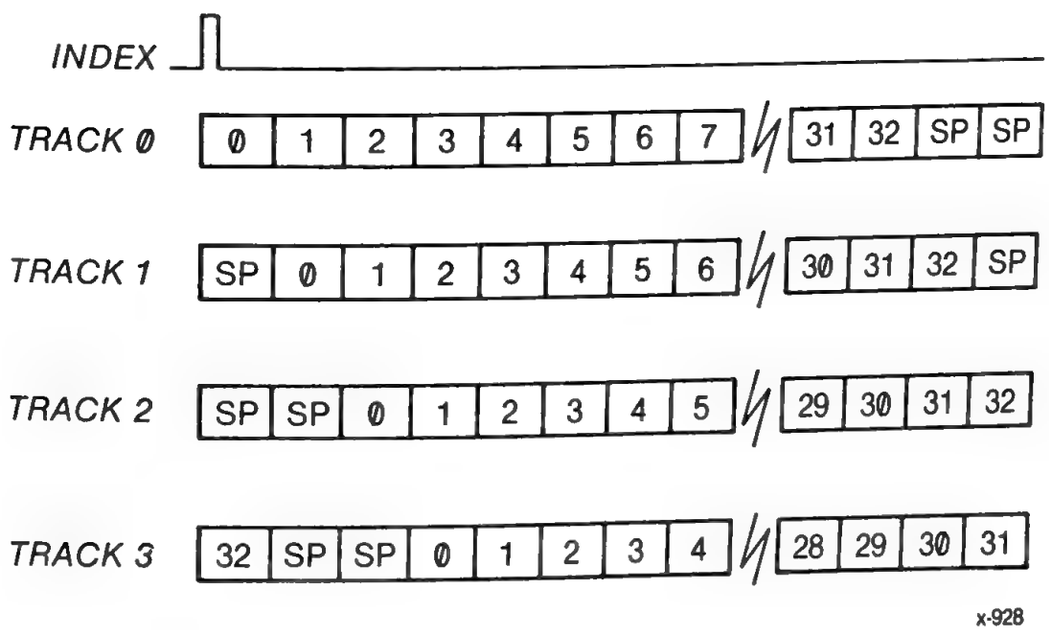

Figure 5-6. Adaptive Format

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CHAPTER 6
INTERFACING INFORMATION

6.1 INTRODUCTION

The following tables provide the MULTIBUS and Storage Module Device (SMD) Interface Signals for use in installing and maintaining your iSBC 226 SMD Disk Controller Board. Included in the tables are the mnemonic, connector and pin number, and description of the interface signals.

Table 6-1. MULTIBUS® Interface Signals

Mnemonic	Conn.	Pin	Used by iSBC® 226 board	Description
ADRØ/	P1	57	Y	
ADR1/	P1	58	Y	
ADR2/	P1	55	Y	
ADR3/	P1	56	Y	
ADR4/	P1	53	Y	
ADR5/	P1	54	Y	
ADR6/	P1	51	Y	
ADR7/	P1	52	Y	
ADR8/	P1	49	Y	
ADR9/	P1	5Ø	Y	
ADRA/	P1	47	Y	
ADRB/	P1	48	Y	
ADRC/	P1	45	Y	
ADRD/	P1	46	Y	Address Bus
ADRE/	P1	43	Y	
ADRF/	P1	44	Y	
ADR1Ø/	P1	28	Y	
ADR11/	P1	3Ø	Y	
ADR12/	P1	32	Y	
ADR13/	P1	34	Y	
ADR14/	P1	57	P	
ADR15/	P1	58	P	Address Bus
ADR16/	P1	55	P	
ADR17/	P1	56	P	

----------(continued)----------

Table 6-1. MULTIBUS® Interface Signals (continued)

Mnemonic	Conn.	Pin	Used by iSBC® 226 board	Description
DATØ/	P1	73	Y	
DAT1/	P1	74	Y	
DAT2/	P1	71	Y	
DAT3/	P1	72	Y	
DAT4/	P1	69	Y	
DAT5/	P1	7Ø	Y	
DAT6/	P1	67	Y	
DAT7/	P1	68	Y	
DAT8/	P1	65	Y	Data Bus
DAT9/	P1	66	Y	
DATA/	P1	63	Y	
DATB/	P1	64	Y	
DATC/	P1	61	Y	
DATD/	P1	62	Y	
DATE/	P1	59	Y	
DATF/	P1	6Ø	Y	
STROBE				
IORC/	P1	21	Y	I/O Read Cmd
IOWC/	P1	22	Y	I/O Write Cmd
MRDC/	P1	19	Y	Mem Read Cmd
MWTC/	P1	2Ø	Y	Mem Write Cmd
XACK/	P1	23	Y	XFER Acknowledge
CLOCKS				
BCLK/	P1	13	P	Bus Clock
CCLK/	P1	31	N	Constant Clock
PLC/	P2	31	N	Power Line Clock
INTERRUPTS				
INTØ/	P1	41	P	
INT1/	P1	42	P	
INT2/	P1	39	P	
INT3/	P1	4Ø	P	
INT4/	P1	37	P	Interrupt Request Levels
INT5/	P1	38	P	
INT6/	P1	35	P	
INT7/	P1	36	P	
INTA/	P1	33	N	

----------(continued)----------

Table 6-1. MULTIBUS® Interface Signals (continued)

Mnemonic	Conn.	Pin	Used by iSBC® 226 board	Description
DMA				
BPRN/	P1	15	Y	Bus Pri. In
BPRO/	P1	16	Y	Bus Pri. Out
BREQ/	P1	18	P	Bus Request
BUSY/	P1	17	Y	Busy Ready
CBRQ/	P1	29	N	Common Bus Request
MISCELLANEOUS CONTROL				
BHEN/	P1	27	Y	Byte High Enable
BD RESET/	P2	36	N	Board Reset
HALT/	P2	28	N	Bus Master Wait State
INH1/	P1	24	N	Inhib. 1 disable RAM
INIT/	P1	14	Y	Initialize
MISCELLANEOUS				
ACLO/	P2	18	P	AC Low
ALE/	P2	32	N	Bus Master ALE
AUX RESET/	P2	38	N	Reset Switch Reserved
LOCK/	P1	25	N	Inhib. 2 dis. PROM or ROM
MPRO/	P2	2Ø	N	Memory Protect
PAR1/	P2	27	N	Parity 1
PAR2/	P2	29	N	Parity 2
WAIT/	P2	3Ø	N	Bus Master Wait State
POWER				
12VB	P2	11,12	N	+12V Battery
5VB	P2	3	N	+5V Battery
GVB	P2	4	N	Return
-12VB	P2	15,16	N	-12V Battery
+5V	P1	3,4,5,6,81, 82,83,84	Y	+5Vdc
+12V	P1	7,8	N	+12Vdc
+15V	P2	23,24	N	+15V
-12V	P1	79,8Ø	P	-12Vdc
-15V	P2	25,26	N	-15V
EEVPP	P2	6	N	E^2 PROM Power
GND	P1	1,2,11,12, 75,76,85,86	Y	Signal GND
GND	P2	1,2,21,22	N	Signal GND

Notes: Y = Yes N = No P = Possibly

Table 6-2. Storage Module Device (SMD) Interface Signals

Name	Cable	Pin+/- CDC	Pin+/- Stnd.	Description
UNIT SELECT				
Unit Select Tag	A	52/22	44/43	Works with Unit Select Bits to initiate a unit select sequence.
Unit Select Bit Ø	A	53/23	46/45	Binary weighted signals to determine one of 16 drives to be selected.
Unit Select Bit 1	A	54/24	48/47	
Unit Select Bit 2	A	56/26	52/51	
Unit Select Bit 3	A	57/27	54/53	
Open Cable Det.	A	44/14	28/27	A signal the controller can use to de-select the drive in event of power failure.
Unit Selected	B	Ø9/22	17/18	A "B" cable signal indicating drive has been selected.
Unit Ready	A	49/19	38/37	The selected drive is up to speed and the heads are loaded, and not faulted.
CONTROL				
Tag 1	A	31/Ø1	Ø2/Ø1	Cylinder select tag causes the drive to seek to the cylinder selected by Bus Bits Ø-1Ø.
Tag 2	A	32/Ø1	Ø4/Ø3	Head Select Tag causes the drive to select the head specified by Bus Bits Ø-9.
Tag 3	A	33/Ø3	Ø6/Ø5	Control Tag commands the drive to perform the function defined by Bus Bits Ø-9.
Pwr. Seq. Hold	A	59	58	Used for power sequencing with Remote/Local.
Sequence Pick In	A	29	57	Used for power sequencing with Remote/Local.
Bus Bit Ø	A	34/Ø4	Ø8/Ø7	Write Gate Enable or bit Ø of head or cyl.
Bus Bit 1	A	35/Ø5	1Ø/Ø9	Read Gate Enable or bit 1 of head or cyl.
Bus Bit 2	A	36/Ø6	12/11	Servo Offset +, or bit 2 of head or cyl.
Bus Bit 3	A	37/Ø7	14/13	Servo Offset -, or bit 3 of head or cyl.

----------(continued)----------

Table 6-2. Storage Module Device (SMD) Interface Signals (continued)

Name	Cable	Pin+/- CDC	Pin+/- Stnd.	Description
CONTROL (continued)				
Bus Bit 4	A	38/Ø8	16/15	Fault Clear, or bit 4 of head or cyl.
Bus Bit 5	A	39/Ø9	18/17	Address mark Enable, or bit 5 of head or cyl.
Bus Bit 6	A	4Ø/1Ø	2Ø/19	Recalibrate, or bit 6 of head or cyl.
Bus Bit 7	A	41/11	22/21	Data Strobe Early, or bit 7 of head or cyl.
Bus Bit 8	A	42/12	24/23	Data Strobe Late, or bit 8 of head or cyl.
Bus Bit 9	A	43/13	26/25	Release, or bit 9 of head or cyl.
Bus Bit 1Ø	A	6Ø/3Ø	6Ø/59	Bit 1Ø of cylinder address.
CLOCKS and DATA				
Index	A	48/18	36/35	A pulse for every index mark.
Read Clock	A	17/Ø5	Ø8/Ø9	Clock to synchronize Read Data.
Read Data	A	16/Ø3	Ø6/Ø5	Read data from drive.
Sector	A	55/25	5Ø/49	Pulse for every sector except during index.
Servo Clock	B	14/Ø2	Ø2/Ø3	Clock to synchronize write data to.
Write Clock	B	19/Ø6	12/11	Clock sent to drive with synchronized write data.
Write Data	B	2Ø/Ø8	14/15	Write data sent to drive.
STATUS				
Address Mark	A	5Ø/2Ø	39/4Ø	Signal indicates if drive has found a sector mark. This is not used by the iSBC 226 board.
Busy	A	51/21	42/41	Indicates that a dual ported drive is busy to the other port.

(continued)

Table 6-2. Storage Module Device (SMD) Interface Signals (continued)

Name	Cable	Pin+/- CDC	Pin+/- Stnd.	Description
STATUS (continued)				
Fault	A	45/15	3Ø/29	Signal indicates if drive is faulted.
On Cylinder	A	47/17	34/33	Signal indicates if drive is on cylinder.
Seek End	B	23/1Ø	2Ø/19	Signal indicates that the drive has completed its commanded seek or the heads have just loaded.
Seek Error	A	46/16	32/31	Signal indicates if drive had a seek error.
Write Protect	A	58/28	56/55	Signal indicates if drive is write protected.

***

CHAPTER 7
SERVICE INFORMATION

7.1 INTRODUCTION

This chapter provides service and repair assistance information, and a board layout diagram for the iSBC 226 SMD Disk Controller Board.

7.2 SERVICE AND REPAIR ASSISTANCE

United States customers can obtain service and repair assistance by contacting Intel Customer Support Marketing Administration in Phoenix, Arizona. Customers outside the United States should contact their sales source (Intel Sales Office or Authorized Distributor) for detailed service information and repair assistance.

Before calling Intel Customer Support Marketing Administration, you should have the following information available:

a. Date you received the product.

b. Complete part number of the product (including dash number). On boards, this number is usually silk-screened onto the board. On other products, it is usually stamped on a label.

c. Serial number of product. On boards, this number is usually stamped on the board. On other products, the serial number is usually stamped on a label.

d. Shipping and billing addresses.

e. If your Intel product warranty has expired, you must provide a purchase order number for billing purposes.

f. If you have an extended warranty agreement, be sure to advise the Customer Support personnel of this agreement.

Use the following telephone numbers for contacting Intel Customer Support Marketing Administration:

Western Region	(6Ø2) 869 - 4951
Midwestern Region	(6Ø2) 869 - 4392
Eastern Region	(6Ø2) 869 - 4Ø45
International	(6Ø2) 869 - 4862

Always contact the Customer Support Marketing Administration Group before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If you are returning the product because of damage sustained during shipment or if the product is out of warranty, a purchase order is required before Intel can initiate the repair.

In preparing the product for shipment to the Repair Center, use the original factory packing material, if possible. If this material is not available, wrap the product in a cushioning material such as Air Cap TH - 24Ø, manufactured by the Sealed Air Corporation, Hawthorne, N.J. Then enclose in a heavy duty corrugated shipping carton, and label "FRAGILE" to ensure careful handling. Ship only to the address specified by the Customer Support Marketing Administration personnel.

7.3 iSBC® 226 BOARD LAYOUT DIAGRAM

Figure 7-1. shows the board layout diagram.

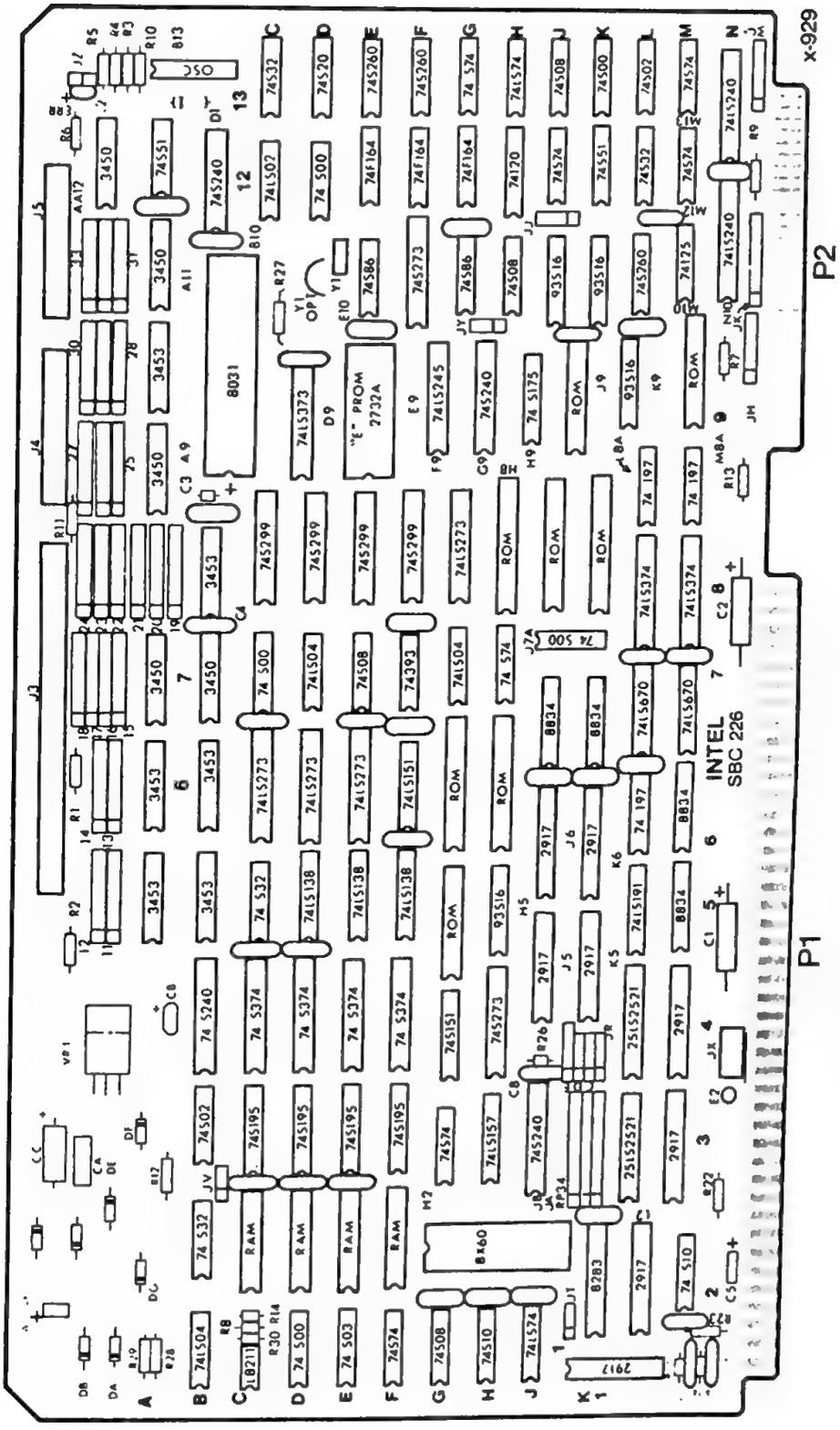

Figure 7-1. iSBC® 226 Board Layout Diagram

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APPENDIX A
FACTORY DEFAULT JUMPER INFORMATION

A.1 INTRODUCTION

This appendix covers the factory configured jumpers (non-user configurable), the factory default jumpers (user-configurable), and the jumper and connector location diagram (Figure A-1.).

A.2 iSBC® 226 BOARD FACTORY CONFIGURED JUMPERS

There are several jumpers on the iSBC 226 board which should not be altered since they are configured for factory use only. Most of these jumpers are hard wired, not removable jumper blocks.

Table A-1. iSBC® 226 Board Factory Configured Jumpers

Jumper	Status	Description
JY2-JY3	In	Closes ECC feedback loop
JY1-JY2	Out	
JJ1-JJ2	Out	Selects Clock for disk sequencer
JJ3-JJ4	In	
JH5-JH6	In	Selects clock for DMA sequencer
JH3-JH4	Out	
JZ1-JZ2	In	Enables crystal clock
JT1-JT2	Out	Buffer Memory Configuration
JT2-JT3	In	
JV2-JV3	In	
JV1-JV2	Out	

A.3 iSBC® 226 BOARD FACTORY DEFAULT JUMPERS

Table A-2. lists the factory default jumpers that are user-configurable. Refer to Chapter 2 (Board Configuration) for more information on jumper options.

Table A-2. iSBC® 226 Board Factory Default Jumpers

Jumper	Status	Description
JA1Ø-JB1Ø	Out	16-Bit Address
JM1-JM2	Out	16-, 2Ø-Bit Address Relocation
JM3-JM4	In	
JA2-JB2	In	I/O Port Default Base Address (Ø1ØØH)
JA4-JB4	In	
JA5-JB5	In	
JA6-JB6	In	
JA7-JB7	In	
JA8-JB8	In	
JA9-JB9	In	
JC1-JD1	In	
JC2-JD2	In	
JC3-JD3	In	
JC4-JD4	In	
JE4-JE5	In	
JM5-JM6	In	ADR14H (Upper Four Address Lines)
JK5-JK6	In	ADR15H
JK1-JK2	In	ADR16H
JK3-JK4	In	ADR17H
JX3-Stake Pin E2	In	Interrupt Request Level 5 (INT 5/)
JE1-JE2	In	Serial DMA Arbitration
JH1-JH2	Out	Power Fail Warning
JN1-JN2	Out	Remote Activity Indicator

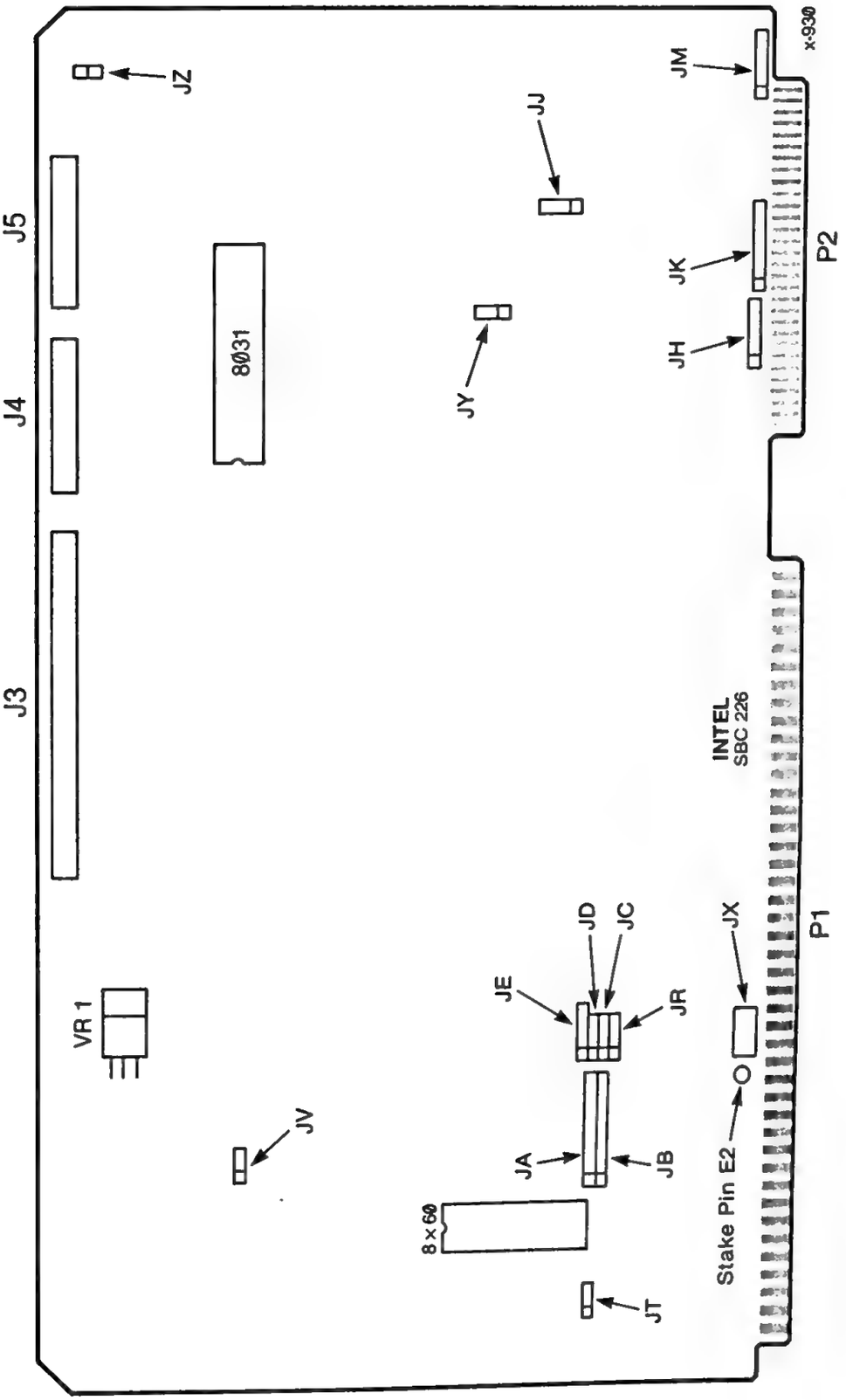


Figure A-1. iSBC® 226 Board Jumper and Connector Diagram

***

INDEX

Primary references are underscored.

***

ERRATA

11/84

iSBC® 226 Storage Module Device (SMD)
Disk Controller Board
Hardware Reference Manual

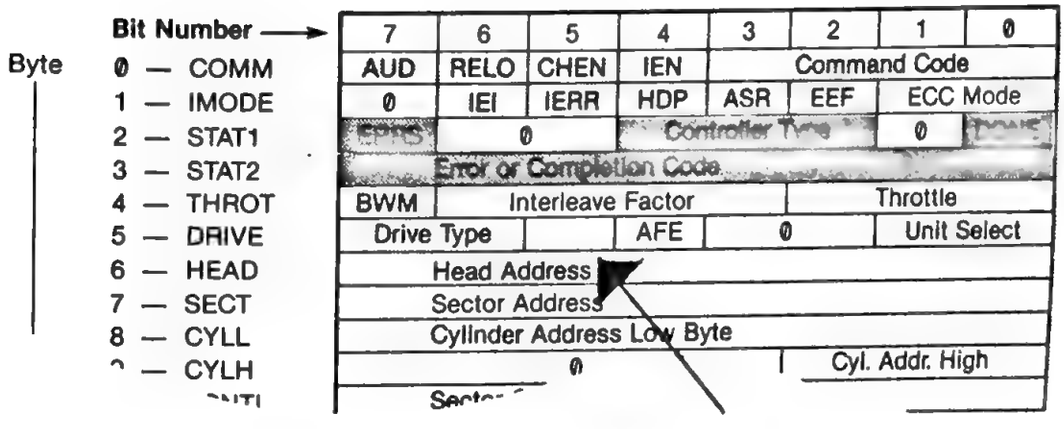
Order Number: 147Ø47-ØØ1

Intel Corporation, 3Ø65 Bowers Avenue, Santa Clara, California 95Ø51

The following changes and improvements were noted after the manual went to press. Please take a few moments to note them on the pages that are affected in the body of the manual.

pg. 5-2 Figure 5-1. Example of Input/Output Parameter Block (IOPB)

CLARIFICATION:
Bit 5 of Byte 5 of the IOPB is empty. This bit is a "Don't Care" condition. This holds true for all the IOPB artwork in this manual.



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